PI7C8954

PCI Quad UART

Datasheet
Revision 1.3
December 2016

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REVISION HISTORY

Date	Revision Number	Description
09/12/14	0.1	Preliminary Datasheet
12/09/15	1.0	Updated Section 1 Feature Updated Section 6.3 Configuration Registers Updated Section 9 Electrical Specification
01/06/16	1.1	Updated Section 9 Electrical Specification Updated Section 11 Ordering Information
08/25/16	1.2	Updated Section 4 Pin Assignment Updated Section 11 Ordering Information
12/02/16	1.3	Updated Section 4 Pin Assignment Updated Section 9 Electrical Specification

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1. FEATURES

- Four high performance 950-class UARTs
- Universal PCI Bus Buffers – Auto sense 3.3V or 5V operation
- 32-bit PCI Bus 2.3 target signaling compliance
- Fully 16C550 software compatible UARTs
- 128-byte FIFO for each transmitter and receiver
- Baud rate up to 15 Mbps in asynchronous mode
- Flexible clock prescaler from 4 to 46
- Data Transfer in Byte, Word and Double-word
- Data Read/Write Burst Operation
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Detection of bad data in the receiver FIFO
- Data framing size including 5, 6, 7, 8 and 9 bits
- Infrared (IrDA 1.0/1.1) Data Encoder/Decoder
- Auto RS-485 Half-duplex Output with Control Polarity Selector
- Eight General Purpose Inputs/Outputs
- A General Purpose 16-bit Timer/Counter
- Hardware reconfiguration through Microwire compatible EEPROM
- Operations via I/O or memory mapping
- Sleep Mode with Automatic Wake-up
- Dual power operation (3.3V or 5.0V for PCI I/O and 1.8V-5.0V for UART I/O)
- Power dissipation: 0.2W typical in normal mode
- Industrial Temperature Range -40^{o} to 85^{o}
- 144-pin LQFP package

2. APPLICATIONS

- Remote Access Servers
- Network / Storage Management
- Factory Automation and Process Control
- Instrumentation
- Multi-port RS-232/ RS-422/ RS-485 Cards
- Point-of-Sale Systems (PoS)
- Industrial PC (IPC)
- Industrial Control
- Gaming Machines
- Building Automation
- Embedded Systems

3. GENERAL DESCRIPTION

The PI7C8954 is a PCI Quad UART (Universal Asynchronous Receiver-Transmitters) I/O Bridge. It is specifically designed to meet the latest system requirements of high performance and lead (Pb) -free. The bridge can be used in a wide range of applications such as Remote Access Servers, Automation, Process Control, Instrumentation, POS, ATM and Multi-port RS232/ RS422/ RS485 Cards. The bridge supports four high performance UARTs, each of which supports Baud rate up to 15 Mbps in asynchronous mode. The UARTs support in-band and out-band auto flow control, arbitrary trigger level, I/O mapping and memory mapping, IrDA (Infrared Data Association) encoder/decoder, 8 general purpose I/O and 16-bit timer counter. The PI7C8954 is fully software compatible with 16C550 type device drivers and can be configured to fit the requirements of RS232, RS422 and RS485 applications. The EEPROM interface is provided for system implementation convenience. Some registers can be pre-programmed via hardware pin settings to facilitate system initialization. For programming flexibility, all of the default configuration registers can be overwritten by EEPROM data, such as sub-vendor and sub-system ID.

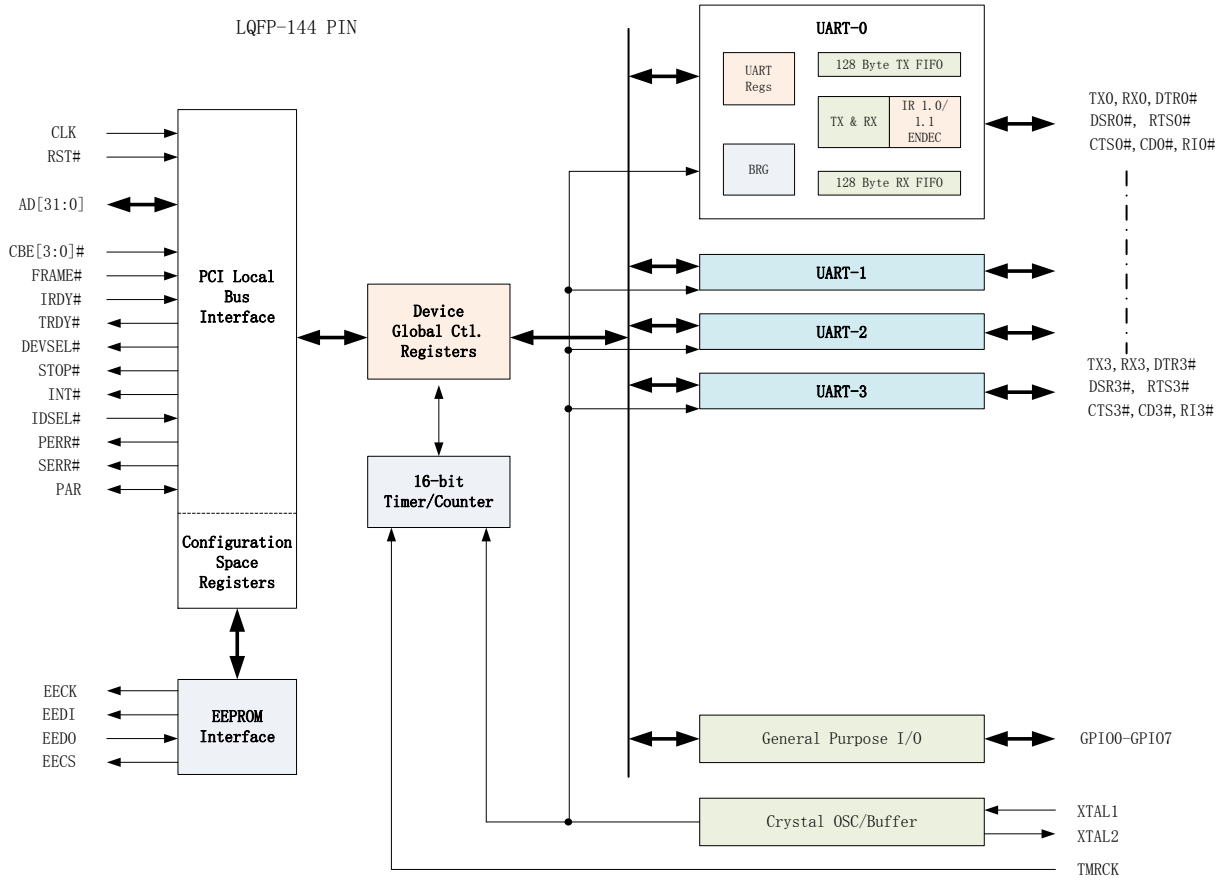


Figure 3-1 PI7C8954 Block Diagram

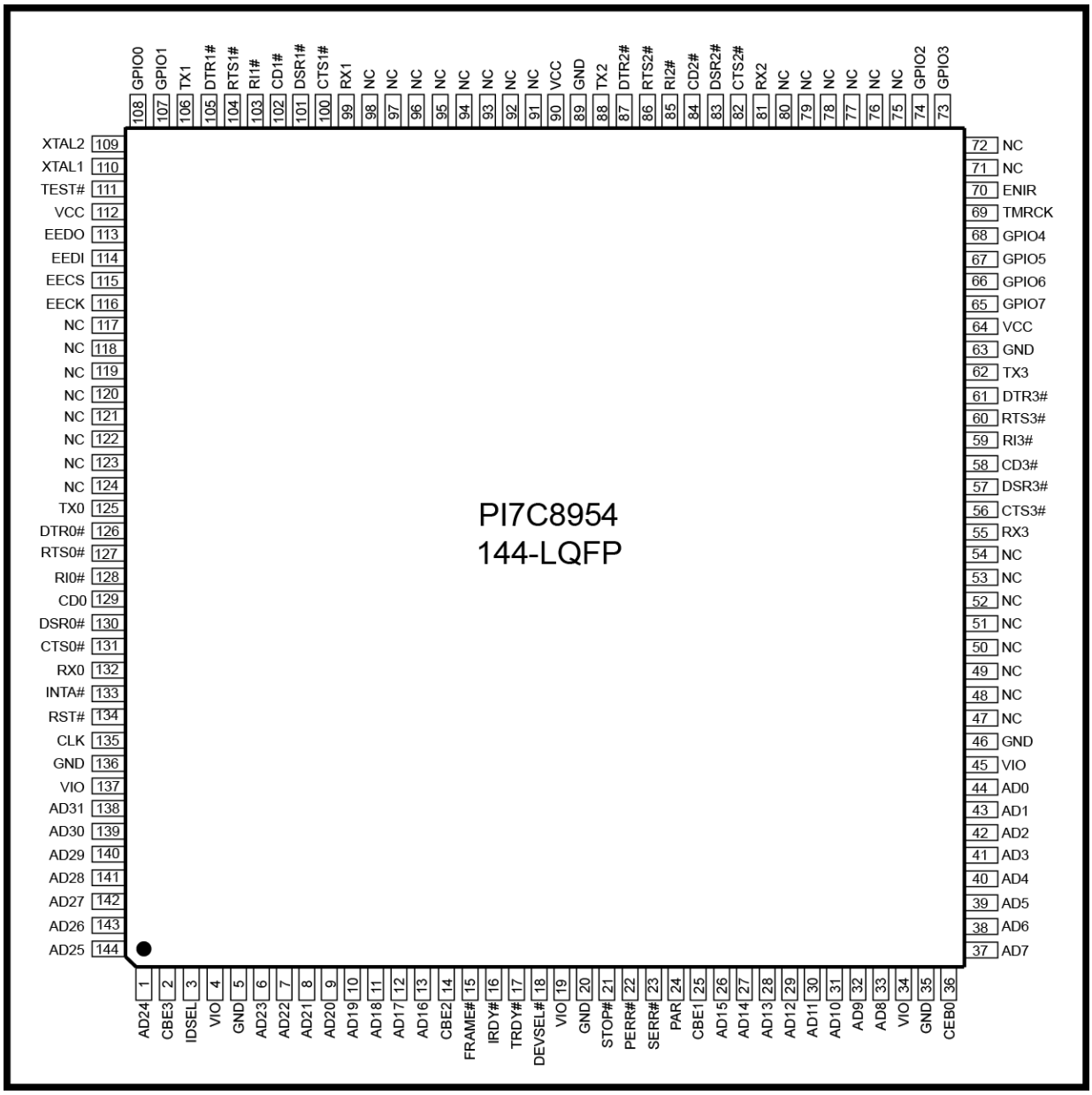


Figure 3-2 Pin Out

4. PIN ASSIGNMENT

NAME	PIN#	TYPE	DESCRIPTION
PCI LOCAL BUS INTERFACE			
RST#	134	I	PCI Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition.
CLK	135	I	PCI Bus clock input of up to 33.34MHz.
AD31-AD25, AD24, AD23-AD16, AD15-AD8, AD7-AD0	138-144, 1, 6-13 26-33 37-44	I/O	Address data lines [31:0] (bidirectional).
FRAME#	15	I	Bus transaction cycle frame (active low). It indicates the beginning and duration of an access.
C/BE3#-C/BE0#	2,14,25,36	I	Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enable during the data phase.
IRDY#	16	I	Initiator Ready (active low). During a write, it indicates valid data is present on data bus. During a read, it indicates the master is ready to accept data.
TRDY#	17	O	Target Ready (active low).
STOP#	21	O	Target request to stop current transaction (active low).
IDSEL	3	I	Initialization device select (active high).
DEVSEL#	18	O	Device select to the PI7C8954 (active low).
INTA#	133	OD	Device interrupt from PI7C8954 (open drain, active low).
PAR	24	I/O	Parity is even across AD[31:0] and C/BE[3:0]# (bidirectional, active high).
PERR#	22	O	Parity error indicator to host (active low). Optional in bus target application.
SERR#	23	OD	System error indicator to host (open drain, active low). Optional in bus target application.
MODEM OR SERIAL I/O INTERFACE			
TX0	125	O	UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX0	132	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by SFR[3].
RTS0#	127	O	UART channel 0 Request to Send or general purpose output (active low).
CTS0#	131	I	UART channel 0 Clear to Send or general purpose input (active low).
DTR0#	126	O	UART channel 0 Data Terminal Ready or general purpose output (active low).
DSR0#	130	I	UART channel 0 Data Set Ready or general purpose input (active low).
CD0#	129	I	UART channel 0 Carrier Detect or general purpose input (active low).
RI0#	128	I	UART channel 0 Ring Indicator or general purpose input (active low).
TX1	106	O	UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX1	99	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by SFR[3].
RTS1#	104	O	UART channel 1 Request to Send or general purpose output (active low).
CTS1#	100	I	UART channel 1 Clear to Send or general purpose input (active low).
DTR1#	105	O	UART channel 1 Data Terminal Ready or general purpose output (active low).
DSR1#	101	I	UART channel 1 Data Set Ready or general purpose input (active low).
CD1#	102	I	UART channel 1 Carrier Detect or general purpose input (active low).
RI1#	103	I	UART channel 1 Ring Indicator or general purpose input (active low).
TX2	88	O	UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX2	81	I	UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by SFR[3].
RTS2#	86	O	UART channel 2 Request to Send or general purpose output (active low).
CTS2#	82	I	UART channel 2 Clear to Send or general purpose input (active low).
DTR2#	87	O	UART channel 2 Data Terminal Ready or general purpose output (active low).
DSR2#	83	I	UART channel 2 Data Set Ready or general purpose input (active low).
CD2#	84	I	UART channel 2 Carrier Detect or general purpose input (active low).
RI2#	85	I	UART channel 2 Ring Indicator or general purpose input (active low).
TX3	62	O	UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.

NAME	PIN#	TYPE	DESCRIPTION
RX3	55	I	UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by SFR[3].
RTS3#	60	O	UART channel 3 Request to Send or general purpose output (active low).
CTS3#	56	I	UART channel 3 Clear to Send or general purpose input (active low).
DTR3#	61	O	UART channel 3 Data Terminal Ready or general purpose output (active low).
DSR3#	57	I	UART channel 3 Data Set Ready or general purpose input (active low).
CD3#	58	I	UART channel 3 Carrier Detect or general purpose input (active low).
RI3#	59	I	UART channel 3 Ring Indicator or general purpose input (active low).
ANCILLARY SIGNALS			
GPIO0	108	I/O	Multi-purpose input/output 0. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO1	107	I/O	Multi-purpose input/output 1. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO2	74	I/O	Multi-purpose input/output 2. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO3	73	I/O	Multi-purpose input/output 3. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO4	68	I/O	Multi-purpose input/output 4. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO5	67	I/O	Multi-purpose input/output 5. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO6	66	I/O	Multi-purpose input/output 6. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT.
GPIO7/EN485#*	65	I/O	Multi-purpose input/output 7. The function of this pin is defined thru the Configuration Register GPSEL, GPLVL, GPINV, GP3T and GPINT. Global Auto RS485 half-duplex direction control enable (active low). During power up or reset, this pin is sampled and if it is a logic low, all UARTs are set for Auto RS485 Mode. Also, the Auto RS485 bit, SFR[2], is set in all channels. Software can override this pin thereafter and enable or disable it. *EN485# pin function is available when use Diodes' PCI UART driver, if use customer own driver, they should implement this function by themselves.
EECK	116	O	Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID and model number during power up or reset.
EECS	115	O	Chip select to a EEPROM device like 93C46. Requires a pull-up 4.7K resistor for external sensing of EEPROM during power up.
EEDI	114	O	Write data to EEPROM device.
EEDO	113	I	Read data from EEPROM device.
XTAL1	110	I	Crystal of up to 24MHz or external clock input of up to 50MHz for data rates up to 6.25Mbps at 5V and 8X sampling. See AC Characterization table. Caution: this input is not 5V tolerant at 3.3V.
XTAL2	109	O	Crystal or buffered clock output.
TMRCK	69	I	16-bit timer/counter external clock input.
ENIR	70	I	Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register SFRST). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART. Software can override this pin thereafter and enable or disable it.
TEST#	111	I	Factory Test. Connect to VCC for normal operation.
VCC	64, 90, 112	PWR	Power supply for non-PCI signals and core logic. it can be 1.8V to 5.0V, no matter if VIO is 3.3V or 5.0V. However VCC must equal VIO at sleep mode to minimize the power current.
VIO	4, 19, 34, 45, 137	PWR	PCI bus I/O power supply - 3.3V or 5V, detected by the auto-sense circuitry of the PI7C8954. This power supply determines the VOH level of the PCI bus interface outputs. (PCI 2.3 signalling compliant at both 3.3V and 5V operation, suitable for universal form factor add-in card application.)
GND	5, 20, 35, 46, 63, 89, 136	PWR	Power supply common, ground.
NC	47-54, 71, 72, 75-80, 91-98, 117-124		No Connection. These pins are reserved and used by the octal PCI UARTs PI7C8958.

NOTE: Pin Type: I = Input, O = Output, I/O = Input/Output, OD = Output Open Drain

5. FUNCTIONAL DESCRIPTION

The PI7C8954 is an integrated solution of four high-performance 16C550 UARTs with one PCI host interface. The PCI interface allows direct access to the configuration and status registers of the UART channels.

The UARTs in the PI7C8954 support the complete register set of the 16C550-type devices. The UARTs support Baud Rates up to 15 Mbps in asynchronous mode. Each UART channel has 128-byte deep transmit and receive FIFOs. The high-speed FIFOs reduce CPU utilization and improve data throughput. In addition, the UARTs support enhanced features including automated in-band flow control using programmable Xon/Xoff in both directions, automated out-band flow control using CTS#/RTS# and/or DRS#/DTR#, and arbitrary transmit and receive trigger levels.

5.1. CONFIGURATION SPACE

The PI7C8954 has two sets of registers to allow various configuration and status monitoring functions. The PCI Configuration Space Registers enable the plug-and-play and auto-configuration when the device is connected to the PCI system bus. The UART configuration and internal registers enable the general UART operation functions, status control and monitoring.

5.1.1. PCI Configuration Space

The PI7C8954 is recognized as a PCI endpoint, which is mapped into the configuration space as a single logical device. Each endpoint in the system, including the PI7C8954, is part of a Hierarchy Domains originated by the Host, which is a tree with a Root Port at its head in the configuration space. The device configuration registers are implemented for the user to access the functionalities provided by the PCI specification.

All PCI endpoints facilitate a PCI-compatible configuration space to maintain compatibility with PCI software configuration mechanism. PCI Local Bus Specification, Revision 3.0 allocates 256 bytes per device function. The user can access the PCI 3.0 compatible region either by conventional PCI 3.0 configuration addresses

5.1.2. UART Configuration Space

Through the UART registers, the user can control and monitor various functionalities of the UARTs on the PI7C8954 including FIFOs, interrupt status, line status, modem status and sample clock. Each of the UART's transmitter and receive data FIFOs can be conveniently accessed by reading and writing the registers in the UART configuration space. These registers allow flexible programming capability and versatile device operations of the PI7C8954. Each UART is accessed through an 8-byte I/O blocks. The addresses of the UART blocks are offset by the base address referred by the Base Address Register (BAR). The value of the base address is loaded from the I/O or Memory Base Address defined in the PCI configuration space.

The PI7C8954 also supports enhanced features such as Xon/Xoff, automatic flow control, Baud Rate prescaling and various status monitoring. These enhanced features are available through the memory address offset by the BAR in the PCI configuration space.

The basic features available in the registers in I/O mode are also available in the registers in memory-mapping mode. Accesses to these registers are equivalent in these two modes.

The UARTs on the PI7C8954 supports operations in 16C450, 16C550 and 16C950 modes. These modes of

operation are selected by writing the SFR, FCR and EFR registers. The PI7C8954 is backward compatible with these modes of operation.

5.2. DEVICE OPERATION

The PI7C8954 is configured by the Host in the bootstrap process during system start-up. The Host performs bus scans and recognizes the device by reading vendor and device IDs. Upon successful device identification, the system then loads device-specific driver software and allocates I/O, memory and interrupt resources. The driver software allows the user to access the functions of the device by reading and writing the UART registers. The PCI interface incorporates convenient device operation and high system performance.

5.2.1. Configuration Access

The PI7C8954 accepts type 0 configuration read and write accesses defined in the PCI 3.0 Specification.

5.2.2. I/O Reads/Writes

The PCI interface of the PI7C8954 decodes incoming transaction packets. If the address is within the region assigned by the I/O Base Address Registers, the transaction is recognized as an I/O Read or Write.

5.2.3. Memory Reads/Writes

Similar to the I/O Read/Write, if the address of the transaction packet is within the memory range, a Memory Read/Write occurs.

5.2.4. Mode Selection

All of the internal UART channels in the I/O Bridge support the 16C450, 16C550, Enhanced 16C550, and Enhanced 950 UART Modes. The mode of the UART operation is selected by toggling the Special Function Register (SFR[5]) and Enhanced Function Register (EFR[4]). The FIFO depth of each mode and the mode selection is tabulated in the table below.

Table 5-1 Mode Selection

UART Mode	SFR[5]	EFR[4]	FIFO Size
450/550	X	0	1/16
Enhanced 550	0	1	128
Enhanced 950	1	1	128

5.2.5. 450/550 Mode

The 450 Mode is inherently supported when 550 Mode is selected. When in the 450 Mode, the FIFOs are in the “Byte Mode”, which refers to the one-byte buffer in the Transmit Holding Register and the Receive Holding Register in each of the UART channels. When in the 550 Mode, the UARTs support an increased FIFO depth of 16.

When EFR[4] is set to “0”, the SFR[5] is ignored, and the 450/550 Mode is selected.

5.2.6. Enhanced 550 Mode

Setting the SFR[5] to “0” and EFR[4] to “1” enables the Enhanced 550 Mode. The Enhanced 550 Mode further increases FIFO depth to 128.

5.2.7. Enhanced 950 Mode

128-deep FIFOs are supported in the Enhanced 950 Mode. When the Enhanced 950 Mode is enabled, the UART channels support additional features:

- Sleep mode
- Special character detection
- Automatic in-band flow control
- Automatic flow control using selectable arbitrary thresholds
- Readable status for automatic in-band and out-of-band flow control
- Flexible clock prescaler
- Programmable sample clock
- DSR/DTR automatic flow control

5.2.8. Transmit and Receive FIFOs

Each channel of the UARTs consists of 128 bytes of transmit FIFOs and 128 bytes of receive FIFOs, namely the Transmit Holding Registers (THR) and the Receive Holding Registers (RHR). The FIFOs provide storage space for the data before they can be transmitted or processed. The THR and RHR operate simultaneously to transmit and read data.

The transmitter reads data from the THR into the Transmit Shift Register (TSR) and removes the data from top of the THR. It then converts the data into serial format with start and stop bits and parity bits if required. If the transmitter completes transmitting the data in the TSR and the THR is empty, the transmitter is in the idle state. The data that arrive most recently are written to the bottom of the THR. If the THR is full, and the user attempts to write data to the THR, a data overrun occurs and the data is lost.

The receiver writes data to the bottom of the RHR when it finishes receiving and decoding the data bits. If the RHR is full when the receiver attempts to write data to it, a data overrun occurs. Any read operation to an empty RHR is invalid.

The empty and full status of the THR and RHR can be determined by reading the empty and full flags in the Line Status Register (LSR). When the transmitter and receiver are ready to transfer data to and from the FIFOs, interrupts are raised to signal this condition. Additionally, the user can use the Receive FIFO Data Counter (RFDC) and Transmit FIFO Data Counter (TFDC) registers to determine the number of items in each FIFO.

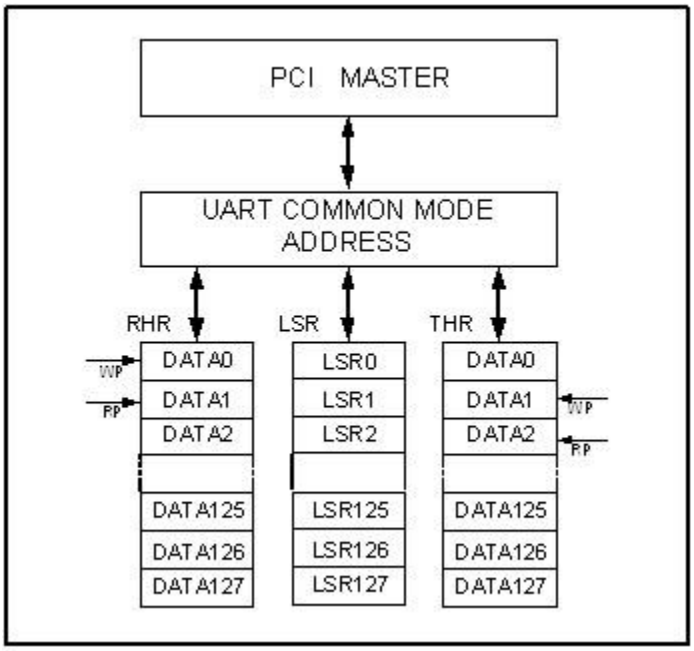


Figure 5-1 Transmit and Receive FIFOs

5.2.9. Automated Flow Control

The device uses automatic in-band flow control to prevent data-overrun to the local receive FIFO and remote receive FIFO. This feature works in conjunction with the special character detection. When an XOFF condition is detected, the UART transmitter will suspend any further data transmission after the current character transmission is completed. The transmitter will resume data-transmission as soon as an XON condition is detected. The automatic in-band feature is enabled by the Enhanced Function Register (EFR). EFR[1:0] enables the in-band receive flow control, and EFR[3:2] enables the in-band transmit flow control.

The out-of-band flow control utilizes RTS# and CTS# pins to suspend and resume the data transmission and to prevent data-overrun. An asserted CTS# pin signals the UART to suspend transmission due to a full remote receive FIFO. Upon detecting an asserted CTS# pin, the UART will complete the current character transmission and enters idle mode until the CTS# pin is deserted.

The UART deasserts RTS# to signal the remote transmitter that the local receive FIFO reaches the programmed upper trigger level. When the local receive FIFO falls below the programmed lower trigger level, the RTS# is reasserted. The automatic out-of-band flow control is enabled by EFR[7:6].

5.2.10. Internal Loopback

The internal loopback capability of the UARTs is enabled by setting Modem Control Register bit-4 (MCR[4]) to 1. When the feature is enabled, the data from the output of the transmit shift register are looped back to the input of the receive shift register. This feature provides the users a way to perform system diagnostics by allowing the UART to receive the same data it is sending.

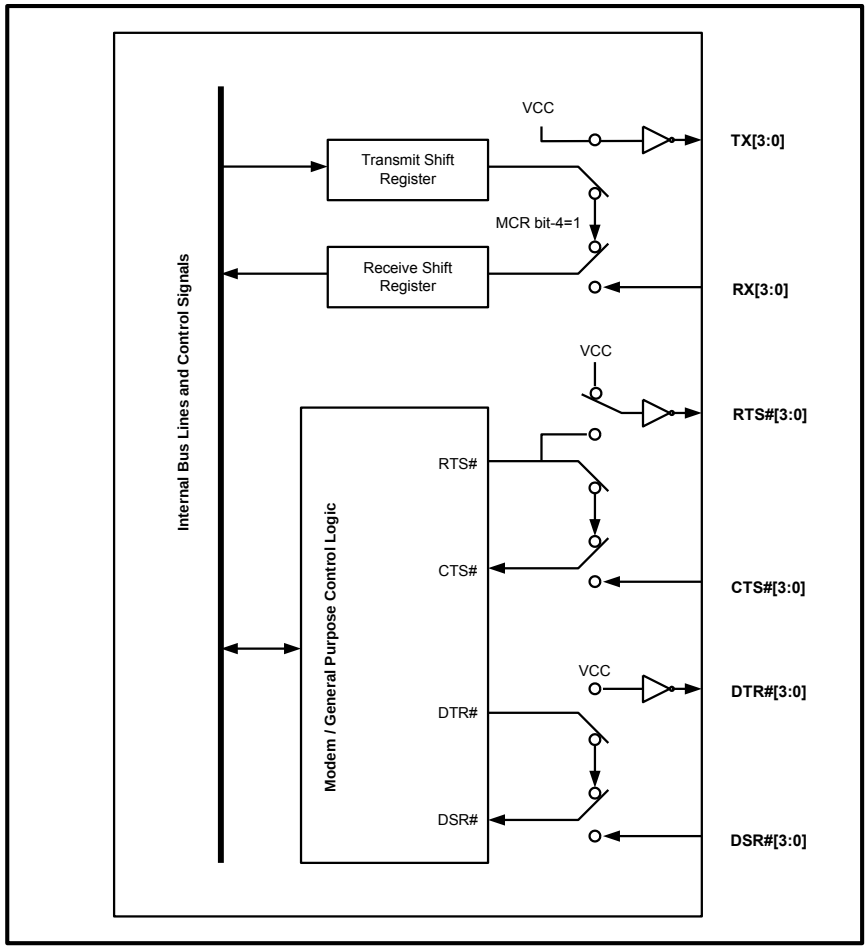


Figure 5-2 Internal Loopback in PI7C8954

5.2.11. Crystal Oscillator

The PI7C8954 uses a crystal oscillator or an external clock source to provide system clock to the Baud Rate Generator. When a clock source is used, the clock signal should be connected to the XTLI pin, and a 2K pull-up resistor should be connected to the XTLO pin.

When a crystal oscillator is used, the XTLI is the input and XTLO is the output, and the crystal should be connected in parallel with two capacitors.

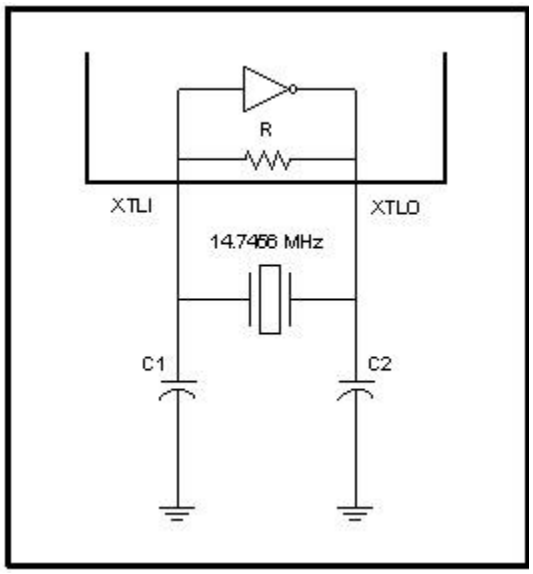


Figure 5-3 Crystal Oscillator as the Clock Source

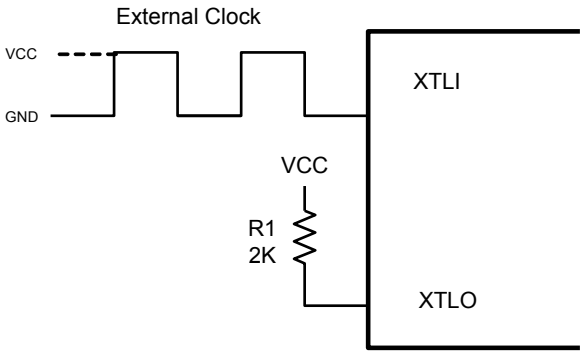


Figure 5-4 External Clock Source as the Clock Source

5.2.12. Baud Rate Generation

The built-in Baud Rate Generator (BRG) allows a wide range of input frequency and flexible Baud Rate generation. To obtain the desired Baud Rate, the user can set the Sample Clock Register (SCR), Divisor Latch Low Register (DLL), Divisor Latch High Register (DLH) and Clock Prescale Registers (CPRM and CPRN). The Baud Rate is generated according to the following equation:

$$BaudRate = \frac{InputFrequency}{Divisor * \Pr escaler}$$

The parameters in the equation above can be programmed by setting the "SCR", "DLL", "DLH", "CPRM" and "CPRN" registers according to the table below.

Table 5-2 Baud Rate Generator Setting

Setting	Description
Divisor	DLL + (256 * DLH)
Prescaler	$2^{M-1} * (SampleClock + N)$
SampleClock	$16 - SCR$, (SCR = '0h' to 'Ch')
M	CPRM, (CPRM = '01h' to '02h')
N	CPRN, (CPRN = '0h' to '7h')

To ensure the proper operation of the Baud Rate Generator, users should avoid setting the value '0' to Sample Clock, Divisor and Prescaler.

The following table lists some of the commonly used Baud Rates and the register settings that generate a specific Baud Rate. The examples assume an Input Clock frequency of 14.7456 Mhz. The SCR register is set to '0h', and the CPRM and CPRN registers are set to '1h' and '0h' respectively. In these examples, the Baud Rates can be generated by different combination of the DLH and DLL register values.

Table 5-3 Sample Baud Rate Setting

Baud Rate	DLH	DLL
1,200	3h	00h
2,400	1h	80h
4,800	0h	C0h
9,600	0h	60h
19,200	0h	30h
28,800	0h	20h
38,400	0h	18h
57,600	0h	10h
115,200	0h	08h
921,600	0h	01h

6. PCI OPERATION

6.1. SUPPORTED PCI TRANSACTION

- Configuration access: The PI7C8954 responds to type 0 configuration reads and writes if the IDSEL signal is asserted and the bus address is selecting function 0 registers. Any other configuration transaction will be ignored.
- I/O read/writes: The address is compared with the addresses reserved in the I/O Base Address Registers (BARs) to decide if the transaction should be ignored (Master abort). Only I/O byte accesses are possible. If multiple bytes is enabled during I/O transaction, only the first byte is valid and all other bytes are ignored.
- Memory reads/writes: The address is compared with the addresses reserved in the Mem Base Address Register. If the memory transaction is targeting to the registers, only first byte is valid and all other bytes are ignored and device will complete the burst transaction as disconnect-with-data. If the memory transaction is targeting to FIFOs, burst (multiple Dword) transaction is supported.
- All other cycles (64-bit, special cycles, reserved encoding etc.) are ignored.
- The PI7C8954 performs medium-speed address decoding as defined by the PCI specification. The Fast back-to-back transactions are supported.
- The PI7C8954 performs parity generation and checking on all PCI bus transactions as defined by PCI spec. If a parity error occurs during the PCI bus address phase, the device will report the error in the standard way by asserting the SERR# bus signal.

6.2. REGISTER TYPES

REGISTER TYPE	DEFINITION
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear

6.3. CONFIGURATION REGISTERS

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Master Latency Timer	Cache Line Size	0Ch
IO BAR Register				10h
MEM BAR Register				14h
Reserved				18h~2Bh
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Capability Pointer				34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – D8h
EEPROM Data		EEPROM Address	EEPROM Control / Status	DCh
Reserved				E0h - FCh

6.3.1. VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

6.3.2. DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this I/O bridge as the PI7C8954. The default value may be changed by auto-loading from EEPROM. Reset to 8954h.

6.3.3. COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.
1	Memory Space Enable	RW	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to response to memory Space accesses. Reset to 0b.
2	Bus Master Enable	RO	It is not implemented. Hardwired to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	Controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI. Must be hardwired to 0b.
8	SERR# enable	RW	This bit, when set, enables the assertion of SERR# when detected System Error by the device. Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of the I/O bridge to generate INTx interrupt Messages. Reset to 0b.
15:11	Reserved	RO	Reset to 00000b.

6.3.4. STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx interrupt Message is pending internally to the device. Reset to 0b.
20	Capabilities List	RO	RO as 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
21	66MHz Capable	RO	Reset to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	RO as 1b.
24	Master Data Parity Error	RWC	It is not implemented. Hardwired to 0b.
26:25	DEVSEL# Timing	RO	Reset to 01b.
27	Signaled Target Abort	RWC	This bit does not apply to UART device.
28	Received Target Abort	RWC	It is not implemented. Hardwired to 0b.
29	Received Master Abort	RWC	Reset to 0b.
30	Signaled System Error	RWC	Reset to 0b.
31	Detected Parity Error	RWC	Reset to 0b.

6.3.5. REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of the I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 00h.

6.3.6. CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 02h to indicate no programming interfaces have been defined for PCI-to-PCI bridges
23:16	Sub-Class Code	RO	Read as 00h to indicate device is PCI-to-PCI bridge
31:24	Base Class Code	RO	Read as 07h to indicate device is a bridge device

6.3.7. CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system to system cache line size. This field is implemented by PCI devices as a RW field for legacy compatibility purposes but has no impact on any PCI device functionality. Reset to 00h.

6.3.8. MASTER LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Latency timer	RO	Does not apply to PCI. Must be hardwired to 00h.

6.3.9. HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 00h to indicate that the register layout conforms to the standard PCI-to-PCI bridge layout. Reset to 00h.
31:24	Reserved	RO	Reset to 00h

6.3.10. BASE ADDRESS REGISTER 0 – OFFSET 10h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 0	RW	Use this I/O base address to map the UART 16550 compatible registers. The base address can be allocated to 64 Bytes. Reset to 00000001h.

6.3.11. BASE ADDRESS REGISTER 1 – OFFSET 14h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 1	RW	Use this memory base address to map the UART 16550 compatible and enhanced registers. The base address can be allocated to 4096 Bytes. Reset to 00000000h

6.3.12. SUBSYSTEM VENDOR REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Sub Vendor ID	RO	Indicates the sub-system vendor id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.3.13. SUBSYSTEM ID REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Sub System ID	RO	Indicates the sub-system device id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.3.14. CAPABILITIES POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capabilities Pointer	RO	This optional register points to a linked list of new capabilities implemented by the device. This default value may be changed by auto-loading from EEPROM. The default value is 00h.
31:8	Reserved	RO	Reset to 000000h.

6.3.15. INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. Reset to 00h.

6.3.16. INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Identifies the legacy interrupt Message(s) the device uses. Reset to 01h.
31:16	Reserved	RO	Reset to 0000h.

6.3.17. EEPROM CONTROL REGISTER – OFFSET DCh

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	Reserved	RO	Reset to 0b.
2	EEPROM Preload Control	RW	Enable preload start. Reset to 0b.
4:3	EEPROM Operation Command	RW	EEPROM Operation Command. 00b: Reserved 01b: Write operation command 10b: Read operation command 11b: Reserved Reset to 00b.
5	Operation Status	RO	When set indicates EEPROM access is ongoing
7:6	Preload Status	RO	EEPROM preload status after finish: 00b: reserved 01b: EEPROM is disabled 10b: EEPROM does not have correct check code 11b: EEPROM data is preloaded normally
15:8	EEPROM Address	RW	EEPROM word address
31:16	EEPROM Write DATA Buffer	RW	EEPROM write data buffer register. Reset to 0000h.

7. UART REGISTER DESCRIPTION

7.1. REGISTER TYPES

REGISTER TYPE	DEFINITION
RO	Read Only
WO	Write Only
RW	Read / Write
WOS	Write 1 to Clear

7.2. REGISTERS IN I/O MODE

Each UART channel has a dedicated 8-byte register block in I/O mode. The register block can be accessed by the UART I/O Base Address, which is obtained by adding the UART Register Offset to the content of the Base Address Register 0 (BAR0). The following diagram shows the arrangement of individual UART register blocks.

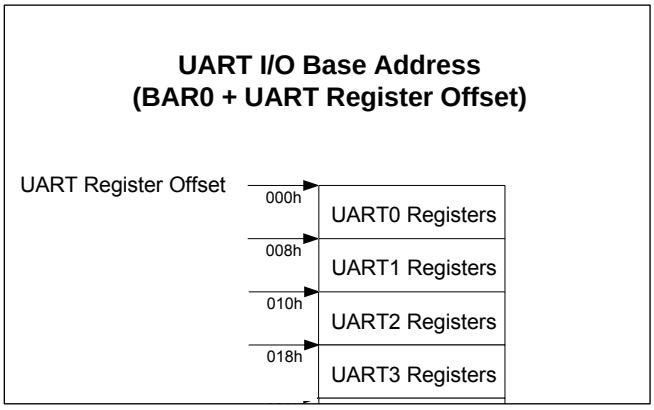


Figure 7-1 UART Register Block Arrangement in I/O Mode

Table 7-1 UART Base Address in I/O Mode

UART	UART I/O Base Address
UART0	BAR0 + 000h
UART1	BAR0 + 008h
UART2	BAR0 + 010h
UART3	BAR0 + 018h

Each register in the UART Register Block can be access by adding an offset to the UART I/O Base Address. The following table lists the arrangement of the registers in the UART Register Block in I/O mode.

Table 7-2 Registers in I/O Mode

Offset	Register Name	Mnemonic	Register Type
UART I/O Base Address + 00h	Receive Holding Register	RHR	RO
UART I/O Base Address + 00h	Transmit Holding Register	THR	WO
UART I/O Base Address + 01h	Interrupt Enable Register	IER	RW
UART I/O Base Address + 02h	Interrupt Status Register	ISR	RO
UART I/O Base Address + 02h	FIFO Control Register	FCR	WO
UART I/O Base Address + 03h	Line Control Register	LCR	RW
UART I/O Base Address + 04h	Modem Control Register	MCR	RW
UART I/O Base Address + 05h	Line Status Register	LSR	RO
UART I/O Base Address + 06h	Modem Status Register	MSR	RO

UART I/O Base Address + 07h	Special Function register	SFR	RW
Additional Standard Registers (Required LCR[7] = 1)			
UART I/O Base Address + 00h	Division Latch Low	DLL	RW
UART I/O Base Address + 01h	Division Latch High	DLH	RW
UART I/O Base Address + 02h	Sample Clock Register	SCR	RW

Addr[5:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x00	RHR	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x00	THR	WO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x01	IER	R/W	0 Reserved	CTS/DSR Int. Enable	RTS/DTR Int. Enable	Xoff/Sp. Char Int. Enable	Modem Status Int. Enable	RX Error Status Int. Enable	TX Empty Int. Enable	RX Data Int. Enable
0x02	ISR	RO	FIOFs Enable	FIOFs Enable	Int.Status Bit-5	Int.Status Bit-4	Int.Status Bit-3	Int.Status Bit-2	Int.Status Bit-1	Int.Status Bit-0
0x02	FCR	WO	RX FIFO Trigger	RX FIFO Trigger	TX FIFO Trigger	TX FIFO Trigger	0 Reserved	TX FIFO Reset	RX FIFO Reset	FIFOs Enable
0x03	LCR	R/W	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length	Word Length
0x04	MCR	R/W	Enhanced TX mode	IrDA Enable	Autoflow Ctl. Enable	Internal Loopback	OP2	OP1	RTS# Pin Control	DTR# Pin Control
0x05	LSR	RO	RX FIFO Error	TSR Empty	THR Empty	RX Break Error	RX Frame Error	RX Parity Error	RX FIFO Overrun	RX Data Ready
0x06	MSR	RO	CD#	RI#	DSR#	CTS#	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#
0x07	SFR	R/W	TFDC/SCR Select	RFDC/LSRC Select	950 Mode Enable	Xon Any	IR Input Invert	Auto RS-485	Auto DSR/DTR	Force TX Enable
0x00	DLL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x01	DLH	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x02	SCR	R/W	0 Reserved	RS-485 9-Bit Mode	RS-485 Invert	IrDA 1.1 FS Mode	Sample Clk Bit-3	Sample Clk Bit-2	Sample Clk Bit-1	Sample Clk Bit-0
Addr[5:0]	**REG**	**R/W**	**Bit-7**	**Bit-6**	**Bit-5**	**Bit-4**	**Bit-3**	**Bit-2**	**Bit-1**	**Bit-0**

Note: DLL,DLH and SCR accessable when LCR[7]=1 only;

7.2.1. RECEIVE HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Rx Holding	RO	When data are read from the Receive Holding Register (RHR), they are removed from the top of the receiver's associated FIFOs, which holds a queue of data received by the receiver. Reset to 00h.

7.2.2. TRANSMIT HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Tx Holding	WO	When data are written to the Transmit Holding Register (THR), they are written to the bottom of the transmitter's associated FIFOs, which holds a queue of data to be transmitted by the transmitter. Reset to 00h.

7.2.3. INTERRUPT ENABLE REGISTER – OFFSET 01h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available Interrupt	RW	0b: Disable the Receive Data Ready Interrupt 1b: Enable the Receive Data Ready Interrupt Reset to 0b.
1	Tx Empty Interrupt	RW	0b: Disable the Transmit Holding Register Empty Interrupt 1b: Enable the Transmit Holding Register Empty Interrupt Reset to 0b.
2	Rx Status Interrupt	RW	0b: Disable the Receive Line Status Interrupt 1b: Enable the Receive Line Status Interrupt Reset to 0b.
3	Modem Status Interrupt	RW	0b: Disable the Modem Status Register Interrupt 1b: Enable the Modem Status Register Interrupt Reset to 0b.
4	Xoff/Special character interrupt	RW	0b: Disable the Software Flow Control Interrupt 1b: Enable the Software Flow Control Interrupt Reset to 0b.
5	RTS Interrupt	RW	0b: Disable RTS/DTR Interrupt 1b: Enable RTS/DTR Interrupt Reset to 0b.
6	CTS Interrupt	RW	0b: Disable CTS/DSR interrupt 1b: Enable CTS/DSR interrupt Reset to 0b.
7	Reserved	RW	Reset to 0b.

7.2.4. INTERRUPT STATUS REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Interrupt Status	RO	0b: An interrupt is pending 1b: No interrupt pending Reset to 1b.
5:1	Encoded Interrupt	RO	Reset to 00h.
7:6	Mirror Bit-0	RO	Reset to 11b.

Priority Level	Interrupt Status Bits								Interrupt Source
	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	0	0	1	1	0	Rx data error
2	0	0	0	0	0	1	0	0	Rx data available
3	0	0	0	0	1	1	0	0	Rx time-out
4	0	0	0	0	0	0	1	0	Tx FIFO empty
5	0	0	0	0	0	0	0	0	Modem status change
6	0	0	0	1	0	0	0	0	Xoff or special character detected
7	0	0	1	0	0	0	0	0	CTS or RTS state

									changed
X	1	1	0	0	0	0	0	1	No interrupt pending

7.2.5. FIFO CONTROL REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION	
0	FIFO Mode Enable	WO	0b: Disable the FIFO mode 1b: Enable the FIFO mode Reset to 0b.	
1	Rx FIFO Flush	WO	0b: No action 1b: Reset the receive FIFO, self-clear after resetting the FIFO Reset to 0b.	
2	Tx FIFO Flush	WO	0b: No action 1b: Reset the transmit FIFO, self-clear after resetting the FIFO Reset to 0b.	
3	Reserved	WO	Reset to 0b.	
5:4	Tx Trigger Level	WO	In the Non-Enhanced mode 00b: 2 01b: 5 10b: 9 11b: 15	In the Enhanced mode 00b: 16 01b: 32 10b: 64 11b: 112
			Reset to 00b.	
7:6	Rx Trigger Level	WO	In the Non-Enhanced mode 00b: 1 01b: 4 10b: 8 11b: 14	In the Enhanced mode 00b: 15 01b: 31 10b: 63 11b: 111
			Reset to 00b.	

7.2.6. LINE CONTROL REGISTER – OFFSET 03h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Data Length	RW	00b: 5-bit data length 01b: 6-bit data length 10b: 7-bit data length 11b: 8-bit data length Reset to 11b.
2	Stop-Bit Length	RW	<table><tr><th>Bit 2 value</th><th>Data length</th><th>Stop bit length</th></tr><tr><td>0</td><td>5,6,7,8</td><td>1</td></tr><tr><td>1</td><td>5</td><td>1.5</td></tr><tr><td>1</td><td>6,7,8</td><td>2</td></tr></table> Reset to 0b.
5:3	Parity Type	RW	<table><tr><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Parity selection</th></tr><tr><td>X</td><td>X</td><td>0</td><td>No parity</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Odd parity</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Even parity</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Mark</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Space</td></tr></table> Reset to 000b.
6	Transmission Break	RW	0b: No transmit break condition 1b: Force the transmitter output to a space for alerting the remote receiver of a line break condition. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Divisor Latch Enable	RW	0b: Data registers are selected 1b: Divisor latch registers are selected Reset to 0b.

7.2.7. MODEM CONTROL REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	DTR Pin Control	RW	0b: Forces DTR output high 1b: Forces DTR output low Reset to 0b.
1	RTS Pin Control	RW	0b: Forces RTS output high 1b: Forces RTS output low Reset to 0b.
2	Output 1	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output1 is routed to RI. Reset to 0b.
3	Output 2	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output2 is routed to DCD. Reset to 0b.
4	Internal Loopback Mode	RW	0b: Disables Internal Loopback Mode 1b: Enables Internal Loopback Mode Reset to 0b.
5	AFE	RW	Autoflow Control Enable. When the AFE is enabled, autoflow control is enabled. When it is disabled, the diagnostic mode is enabled. In the diagnostic mode, transmitted data is immediately received. When AFE is set to "1", MCR Bit 1 is used to enable and disable the auto-RTS. MCR Bit 5 (AFE) / MCR Bit 1 (RTS) / Configuration 1 / 1 / Auto-RTS and auto-CTS are enabled (autoflow control enabled). 1 / 0 / Only auto-CTS is enabled. 0 / x / Auto-RTS and auto-CTS are disabled. Reset to 0b.
6	IrDA Mode	RW	IrDA Mode Enable. 1b: Enables IrDA mode. 0b: Disables IrDA mode. Reset to ENIR pin input.
7	Enhanced Transmission	RW	0b: Insert 1, 1.5 or 2 stop-bits between two transmitted characters. 1b: Insert 0.5 stop-bits between two transmitted characters. Note: Enabling feature may result in certain compatibility issues. This feature is only recommended when using two Pericom UART devices. Reset to 0b.

7.2.8. LINE STATUS REGISTER – OFFSET 05h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	Rx FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	Rx Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.
3	Rx Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	Rx Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	Tx Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 1b.
6	Tx Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 1b.
7	Rx Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.2.9. MODEM STATUS REGISTER – OFFSET 06h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Delta CTS	RO	0b: No change in CTS input. 1b: Indicates the CTS input has changed state. This bit is read-clear. Reset to 0b.
1	Delta DSR	RO	0b: No change in DSR input. 1b: Indicates the DSR input has changed state. This bit is read-clear. Reset to 0b.
2	Trailing RI Edge	RO	0b: No change in RI input 1b: Indicates the RI input has changed state from the logic 0 to the logic 1. This bit is read-clear. Reset to 0b.
3	Delta DCD	RO	0b: No change in DCD input 1b: Indicates the DCD input has changed state. This bit is read-clear. Reset to 0b.
4	CTS	RO	0b: The CTS input state is the logic 0 1b: The CTS input state is the logic 1 Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
5	DSR	RO	0b: The DSR input state is the logic 0 1b: The DSR input state is the logic 1 Reset to 0b.
6	RI	RO	The input state of RI pin Reset to 0b.
7	DCD	RO	The input state of DCD pin Reset to 0b.

7.2.10. SPECIAL FUNCTION REGISTER – OFFSET 07h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Force Transmission	RW	Forces transmitter to always to transmit data. 1b: Enabled 0b: Disabled Reset to 0b.
1	Auto DSR and DTR Flow Control	RW	Auto DSR and DTR flow control enable 1b: Enables DSR and DTR auto flow control 0b: Disables DSR and DTR auto flow control Reset to 0b.
2	Auto RS-485	RW	Auto RS-485 half-duplex direction control mode enable 1b: Enables RS-485 half-duplex direction control mode 0b: Disables RS-485 half-duplex direction control mode Reset to inversed EN485n pin input.
3	IrDA Invert	RW	Infrared RX input logic select 1b: RX input active LOW (Invert mode) 0b: RX input active HIGH (Normal mode) Reset to 0b.
4	Xon Any Mode	RW	Xon Any mode enable 1b: Enables Xon Any mode 0b: Disables Xon Any mode Reset to 0b.
5	950 Mode	RW	950 mode enable 1b: Enables 950 mode 0b: Non-950 mode Reset to 0b.
6	RFD / LSR Counter Select	RW	RFD or LSR counter register select 1b: OFFSET 15 bit[7:0] acts as the Line Status Register Counter 0b: OFFSET 15 bit[7:0] acts as the Receive FIFO Data Counter Reset to 0b.
7	TFD / SCR Select	RW	TFD or SCR register select 1b: OFFSET 16 bit[7:0] acts as the Transmit FIFO Data Counter 0b: OFFSET 16 bit[7:0] acts as the Sample Clock Register Reset to 0b.

7.2.11. DIVISOR LATCH LOW REGISTER – OFFSET 00h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor Low	RW	Lower-part of the divisor register Reset to 00h.

7.2.12. DIVISOR LATCH HIGH REGISTER – OFFSET 01h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor High	RW	Higher-part of the divisor register Reset to 00h.

7.2.13. SAMPLE CLOCK REGISTER – OFFSET 02h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Sample Clock	RW	This register determines the Sample Clock value (SC) used in the Baud Rate Generator. Please refer to 5.2.12 Baud Rate Generation for more detail 0000b: SC = 16 0001b: SC = 15 0010b: SC = 14 0011b: SC = 13 0100b: SC = 12 0101b: SC = 11 0110b: SC = 10 0111b: SC = 9 1000b: SC = 8 1001b: SC = 7 1010b: SC = 6 1011b: SC = 5 1100b: SC = 4 Other settings are reserved. Reset to 0h.
4	IrDA 1.1 Mode	RW	IrDA mode select 1b: Enables IrDA 1.1 mode (Fast mode) 0b: Disable IrDA 1.1 mode (Normal 1.0 mode) Reset to 0b.
5	RS-485 Invert	RW	Auto RS-485 direction control polarity select 1b: RTS# HIGH when transmitting, LOW when receiving 0b: RTS# LOW when transmitting, HIGH when receiving Reset to 0b.
6	RS-485 9-Bit Mode Enable	RW	Auto RS-485 9-bit mode enable 1b: Enables Auto RS-485 9-bit mode. 0b: Disables Auto RS-485 9-bit mode. Reset to 0b.
7	Reserved	RO	Reset to 0b.

7.3. REGISTERS IN MEMORY-MAPPING MODE

Each UART channel has a dedicated 512-byte register block in Memory mode. The register block can be accessed by the UART Memory Base Address, which is obtained by adding the UART Register Offset to the content of the Base Address Register 1 (BAR1). The following diagram shows the arrangement of individual UART register blocks.

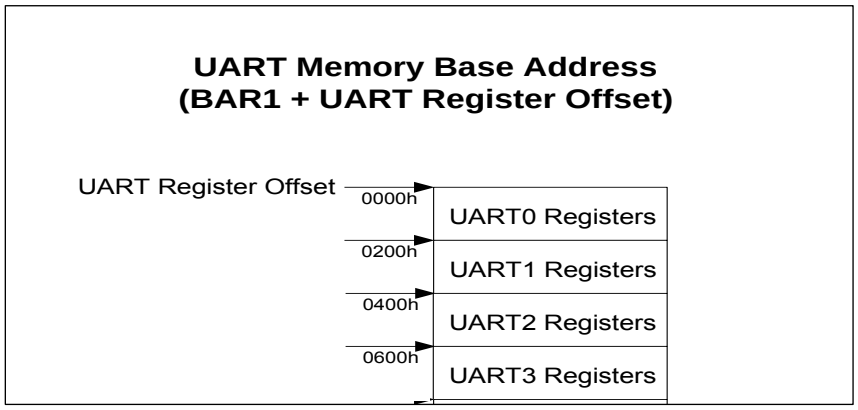


Figure 7-2 UART Register Block Arrangement in Memory Mode

Table 7-3 UART Base Address in Memory Mode

UART	UART I/O Base Address
UART0	BAR1 + 0000h
UART1	BAR1 + 0200h
UART2	BAR1 + 0400h
UART3	BAR1 + 0600h

Each register in the UART Register Block can be access by adding an offset to the UART Memory Base Address. The following table lists the arrangement of the registers in the UART Register Block in memory mode.

Table 7-4 Memory-Map mode

Offset	Register Name	Mnemonic	Register Type
UART Memory Base Address + 00h	Receive Holding Register	RHR	RO
UART Memory Base Address + 00h	Transmit Holding Register	THR	WO
UART Memory Base Address + 01h	Interrupt Enable Register	IER	RW
UART Memory Base Address + 02h	Interrupt Status Register	ISR	RO
UART Memory Base Address + 02h	FIFO Control Register	FCR	WO
UART Memory Base Address + 04h	Line Control Register	LCR	RW
UART Memory Base Address + 04h	Modem Control Register	MCR	RW
UART Memory Base Address + 05h	Line Status Register	LSR	RO
UART Memory Base Address + 06h	Modem Status Register	MSR	RO
UART Memory Base Address + 07h	Special Function Register	SFR	RW
UART Memory Base Address + 08h	Divisor Latch Low	DLL	WO
UART Memory Base Address + 09h	Divisor Latch High	DLH	WO
UART Memory Base Address + 0Ah	Enhanced Function Register	EFR	RW
UART Memory Base Address + 0Bh	XON 1 Character/Special Character 1	XON1	RW
UART Memory Base Address + 0Ch	XON 2 Character/Special Character 2	XON2	RW
UART Memory Base Address + 0Dh	XOFF 1 Character/Special Character 3	XOFF1	RW
UART Memory Base Address + 0Eh	XOFF 2 Character/Special	XOFF2	RW

	Character 3		
UART Memory Base Address + 0Fh	Advanced Status Register	ASR	RW
UART Memory Base Address + 10h	Transmitter Interrupt Trigger Level	TTL	RW
UART Memory Base Address + 11h	Receiver Interrupt Trigger Level	RTL	RW
UART Memory Base Address + 12h	Automatic Flow control lower trigger level	FCL	RW
UART Memory Base Address + 13h	Automatic Flow control lower higher level	FCH	RW
UART Memory Base Address + 14h	Baud rate Prescale	CPR	RW
UART Memory Base Address + 15h	Receive FIFO Data Counter / Line Status Register Counter	RFDC / LSRC	RO
UART Memory Base Address + 16h	Transmit FIFO Data Counter / Sample Clock Register	TFDC / SCR	RW
UART Memory Base Address + 17h	Global Register of LSR	GLSR	RW
UART Memory Base Address + 18h	Global Interrupt Enable Register	GINTE	RW
UART Memory Base Address + 19h	Global Interrupt Status Register	GINTS	RO
UART Memory Base Address + 1Ah	TX Overrun Register	TXOR	RO
UART Memory Base Address + 1Bh	RX Overrun Register	RXOR	RO
UART Memory Base Address + 1Ch	Interrupt Status Register	INTS	RO
UART Memory Base Address + 1Dh	RX FIFO Counter	RXFC	RO
UART Memory Base Address + 1Eh	TX FIFO Counter	TXFC	RO
UART Memory Base Address + 1Fh	FCR Mirror Register	FCRM	RO
UART Memory Base Address + 20h	User Define Timeout Counter Register-1	TCRL	RW
UART Memory Base Address + 21h	User Define Timeout Counter Register-2	TCRH	RW
UART Memory Base Address + 22h	User Define Trigger Level Register	RXTH	RW
UART Memory Base Address + 23h	User Define Register Enable	RTEN	RW
UART Memory Base Address + 24h	TX Idle Counter Register	TIDC	RW
UART Memory Base Address + 25h	TX Idle Counter Enable	TIDE	RW
UART Memory Base Address + 28h	Special Character 1 Register	SCH1	RW
UART Memory Base Address + 29h	Special Character 2 Register	SCH2	RW
UART Memory Base Address + 2Ah	Special Character 3 Register	SCH3	RW
UART Memory Base Address + 2Bh	Special Character 4 Register	SCH4	RW
UART Memory Base Address + 2Ch	Special Character Enable/Clear	SPEC	RW
UART Memory Base Address + 2Dh	FLASH_LSR / TX_EMPTY Interrupt Enable Register	FLSTE	RW
UART Memory Base Address + 2Eh	In BAND Transmit Flow Control	IBTFC	RW
UART Memory Base Address + 2Fh	Advance Control Register	ACR	RW
Offset	**Register Name**	**Mnemonic**	**Register Type**
UART Memory Base Address + 100h ~17Fh	UART Receiver FIFO DATA Register. Use this register to map RX FIFO data content.	RXFIFO	RO
UART Memory Base Address + 100h ~17Fh	UART Transmitter FIFO DATA Register. Use this register to map TX FIFO data content.	TXFIFO	WO
UART Memory Base Address + 180h ~1FFh	UART LSR FIFO DATA Register. Use this register to map LSR FIFO data content	LSFIFO	RO

Table 7-5 Device Configuration Registers Accessible Channel-0 Only

Offset	Register Name	Mnemonic	Register Type
UART Memory Base Address + 40h	Global Interrupt Register 0	INT0	RO
UART Memory Base Address + 41h	Global Interrupt Register 1	INT1	RO
UART Memory Base Address + 42h	Global Interrupt Register 2	INT2	RO
UART Memory Base Address + 43h	Global Interrupt Register 3	INT3	RO
UART Memory Base Address + 44h	Timer Control Register	TICTL	RW
UART Memory Base Address + 46h	Timer/Counter Latch LSB	TILSB	RW
UART Memory Base Address + 47h	Timer/Counter Latch MSB	TIMSB	RW
UART Memory Base Address + 4Ah	Software Reset Register	SFRST	WOS
UART Memory Base Address + 4Bh	Sleep Mode Control Register	SLEEP	RW
UART Memory Base Address + 4Ch	Device Revision Register	DREV	RO

UART Memory Base Address + 4Dh	Device Identification Register	DVID	RO
UART Memory Base Address + 4Eh	Simultaneous Configuration All UART Register	SCWR	RW
UART Memory Base Address + 4Fh	General-purpose IO Interrupt Mask Register	GPINT	RW
UART Memory Base Address + 50h	General-purpose IO Level Control Register	GPLVL	RW
UART Memory Base Address + 51h	General-purpose IO Output Control Register	GP3T	RW
UART Memory Base Address + 52h	General-purpose IO Input Polarity Select Register	GPINV	RW
UART Memory Base Address + 53h	General-purpose IO Select Register	GPSEL	RW

UART Channel Reisters:

Addr[5:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x00	RHR	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x00	THR	WO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x01	IER	R/W	0 Reserved	CTS/DSR Int. Enable	RTS/DTR Int. Enable	Xoff/Sp. Char Int. Enable	Modem Status Int. Enable	RX Error Status Int. Enable	TX Empty Int. Enable	RX Data Int. Enable
0x02	ISR	RO	FIOFs Enable	FIOFs Enable	Int.Status Bit-5	Int.Status Bit-4	Int.Status Bit-3	Int.Status Bit-2	Int.Status Bit-1	Int.Status Bit-0
0x02	FCR	WO	RX FIFO Trigger	RX FIFO Trigger	TX FIFO Trigger	TX FIFO Trigger	0 Reserved	TX FIFO Reset	RX FIFO Reset	FIFOs Enable
0x03	LCR	R/W	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length	Word Length
0x04	MCR	R/W	Enhanced TX mode	IrDA Enable	Autoflow Ctl. Enable	Internal Loopback	OP2	OP1	RTS# Pin Control	DTR# Pin Control
0x05	LSR	RO	RX FIFO Error	TSR Empty	THR Empty	RX Break Error	RX Frame Error	RX Parity Error	RX FIFO Overrun	RX Data Ready
0x06	MSR	RO	CD#	RI#	DSR#	CTS#	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#
0x07	SFR	R/W	TFDC/SCR Select	RFDC/LSR Select	950 Mode Enable	Xon Any	IR Input Invert	Auto RS-485	Auto DSR/DTR	Force TX Enable
0x08	DLL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x09	DLH	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x0A	EFR	R/W	Auto CTS Enable	Auto RTS Enable	Sp. Char Detection	Enhanced Enable	SF Flow Ctl. Bit-3	SF Flow Ctl. Bit-2	SF Flow Ctl. Bit-1	SF Flow Ctl. Bit-0
0x0B	XON1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x0C	XON2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x0D	XOFF1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x0E	XOFF2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x0F	ASR	RO	0 Reserved	0 Reserved	Xoff Detect	Xon Detect	Sp.Char Detect	Xon/Xoff Detect	Remote TX Disable	TX Disable
0x10	TTL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x11	RTL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x12	FCL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x13	FCH	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x14	CPR	R/W	CPRM Bit-4	CPRM Bit-3	CPRM Bit-2	CPRM Bit-1	CPRM Bit-0	CPRN Bit-2	CPRN Bit-1	CPRN Bit-0
0x15	RFDC	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x15	LSRC	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x16	TFDC	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x16	SCR	R/W	0 Reserved	0 Reserved	0 Reserved	0 Reserved	Sample Clk Bit-3	Sample Clk Bit-2	Sample Clk Bit-1	Sample Clk Bit-0
0x17	GLSR	RO	RX Data Error	TSR Empty	THR Empty	RX Break Error	RX Frame Error	RX Parity Error	RX FIFO Overrun	RX Data Ready
0x18	GINTE	R/W	Reserved	Reserved	Reserved	Reserved	Ch-3 EN	Ch-2 EN	Ch-1 EN	Ch-0 EN
0x19	GINTS	RO	Reserved	Reserved	Reserved	Reserved	Ch-3 Int	Ch-2 Int	Ch-1 Int	Ch-0 Int
Addr[5:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

UART Channel Reisters: (Continue)

Addr[5:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x1A	TXOR	RO	TX overrun	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x1B	RXOR	RO	Reserved	Reserved	Reserved	RX overrun	Reserved	Reserved	Reserved	Reserved
0x1C	INTS	RO	RTS/CTS Int	Xoff Int	MS Int	Thre Int	Ti Int	Rda Int	Rls Int	Reserved
0x1D	RXFC	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x1E	TXFC	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x1F	FCRM	RO	RX FIFO Trigger	RX FIFO Trigger	TX FIFO Trigger	TX FIFO Trigger	0 Reserved	TX FIFO Reset	RX FIFO Reset	FIFOs Enable
0x20	TCRL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x21	TCRH	R/W	Reserved	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x22	RXTH	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x23	RTEN	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXTH EN	TIREG EN
0x24	TIDC	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x25	TIDE	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RTOUT EN	TIDLE EN
0x26	RESERV	RO	0	0	0	0	0	0	0	0
0x27	RESERV	RO	0	0	0	0	0	0	0	0
0x28	SCH1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x29	SCH2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x2A	SCH3	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x2B	SCH4	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x2C	SPEC	R/W	SCH4 CLR	SCH3 CLR	SCH2 CLR	SCH1 CLR	SCH4 EN	SCH3 EN	SCH2 EN	SCH1 EN
0x2D	FLSTE	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Flash LSR	TX_Em Int
0x2E	IBTFC	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	T_XON
0x2F	ACR	R/W	0 Reserved	RS-485 9-Bit Mode	RS-485 Invert	IrDA 1.1 FS Mode	0 Reserved	0 Reserved	TX disable	RX disable
Addr[5:0]	**REG**	**R/W**	**Bit-7**	**Bit-6**	**Bit-5**	**Bit-4**	**Bit-3**	**Bit-2**	**Bit-1**	**Bit-0**

FIFOs Data Registers:

Addr[8:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x100-0x17F	RxFIFO Data	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x100-0x17F	TxFIFO Data	WO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x180-0x1FF	LSFIFO Data	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Addr[8:0]	**REG**	**R/W**	**Bit-7**	**Bit-6**	**Bit-5**	**Bit-4**	**Bit-3**	**Bit-2**	**Bit-1**	**Bit-0**

Note: RFDC/LSRC accessable when SFR[6]=0/1;
TFDC/SCR accessable when SFR[7]=1/0.

UART Global Registers: (accessable on UART channel-0 only)

Addr[5:0]	REG	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x40	INT0	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x41	INT1	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x42	INT2	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x43	INT3	RO	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x44	TICTL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x45	RESERV	RO	0	0	0	0	0	0	0	0
0x46	TILSB	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x47	TIMSB	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x48	RESERV	RO	0	0	0	0	0	0	0	0
0x49	RESERV	RO	0	0	0	0	0	0	0	0
0x4A	SFRST	WOS	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x4B	SLEEP	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x4C	DREV	RO	0	0	0	0	0	0	0	1
0x4D	DVID	RO	0	1	0	1	1	0	0	0
0x4E	SCWR	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCWR EN
0x4F	GPINT	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x50	GPLVL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x51	GP3T	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x52	GPINV	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0x53	GPSEL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Addr[5:0]	**REG**	**R/W**	**Bit-7**	**Bit-6**	**Bit-5**	**Bit-4**	**Bit-3**	**Bit-2**	**Bit-1**	**Bit-0**

7.3.1. RECEIVE HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Rx Holding	RO	When data are read from the Receive Holding Register (RHR), they are removed from the top of the receiver's associated FIFOs, which holds a queue of data received by the receiver. Data read from the RHR when the FIFOs are empty are invalid. The Line Status Register (LSR) indicates the full or empty status of the FIFOs. Reset to 00h.

7.3.2. TRANSMIT HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Tx Holding	WO	When data are written to the Transmit Holding Register (THR), they are written to the bottom of the transmitter's associated FIFOs, which holds a queue of data to be transmitted by the transmitter. Data written to the THR when the FIFOs are full are lost. The Line Status Register (LSR) indicates the full or empty status of the FIFOs. Reset to 00h.

7.3.3. INTERRUPT ENABLE REGISTER – OFFSET 01h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available Interrupt	RW	0b: Disable the Receive Data Ready Interrupt 1b: Enable the Receive Data Ready Interrupt Reset to 0b.
1	Tx Empty Interrupt	RW	0b: Disable the Transmit Holding Register Empty Interrupt 1b: Enable the Transmit Holding Register Empty Interrupt Reset to 0b.
2	Rx Error Status	RW	0b: Disable the Receive Line Status Interrupt 1b: Enable the Receive Line Status Interrupt Reset to 0b.
3	Modem Status Interrupt	RW	0b: Disable the Modem Status Register Interrupt 1b: Enable the Modem Status Register Interrupt Reset to 0b.
4	Xoff/Special character interrupt	RW	0b: Disable the Software Flow Control Interrupt 1b: Enable the Software Flow Control Interrupt Reset to 0b.
5	RTS Interrupt	RW	0b: Disable RTS/DTR Interrupt 1b: Enable RTS/DTR Interrupt Reset to 0b.
6	CTS Interrupt	RW	0b: Disable CTS/DSR interrupt 1b: Enable CTS/DSR interrupt Reset to 0b.
7	Reserved	RW	Reset to 0b.

7.3.4. INTERRUPT STATUS REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Interrupt Status	RO	0b: An interrupt is pending 1b: No interrupt pending Reset to 1b.
5:1	Encoded Interrupt	RO	Reset to 00h.
7:6	Mirror Bit-0	RO	Reset to 11b.

Priority Level	Interrupt Status Bits								Interrupt Source
	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	0	0	1	1	0	Rx data error
2	0	0	0	0	0	1	0	0	Rx data available
3	0	0	0	0	1	1	0	0	Rx time-out
4	0	0	0	0	0	0	1	0	Tx FIFO empty
5	0	0	0	0	0	0	0	0	Modem status change
6	0	0	0	1	0	0	0	0	Xoff or special character detected
7	0	0	1	0	0	0	0	0	CTS or RTS state changed
X	1	1	0	0	0	0	0	1	No interrupt pending

7.3.5. FIFO CONTROL REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION
0	FIFO Mode Enable	WO	0b: Disable the FIFO mode 1b: Enable the FIFO mode Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION	
1	Rx FIFO Flush	WO	0b: No action 1b: Reset the receive FIFO, self-clear after resetting the FIFO Reset to 0b.	
2	Tx FIFO Flush	WO	0b: No action 1b: Reset the transmit FIFO, self-clear after resetting the FIFO Reset to 0b.	
3	Reserved	WO	Reset to 0b	
5:4	Tx Trigger Level	WO	In the Non-Enhanced mode 00b: 2 01b: 5 10b: 9 11b: 15	In the Enhanced mode 00b: 16 01b: 32 10b: 64 11b: 112
			Reset to 00b.	
7:6	Rx Trigger Level	WO	In the Non-Enhanced mode 00b: 1 01b: 4 10b: 8 11b: 14	In the Enhanced mode 00b: 15 01b: 31 10b: 63 11b: 111
			Reset to 00b.	

7.3.6. LINE CONTROL REGISTER – OFFSET 03h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Data Length	RW	00b: 5-bit data length 01b: 6-bit data length 10b: 7-bit data length 11b: 8-bit data length Reset to 00b.
2	Stop-Bit Length	RW	<table><tr><td>Bit 2 value</td><td>Data length</td><td>Stop bit length</td></tr><tr><td>0</td><td>5,6,7,8</td><td>1</td></tr><tr><td>1</td><td>5</td><td>1.5</td></tr><tr><td>1</td><td>6,7,8</td><td>2</td></tr></table> Reset to 0b.
5:3	Parity Type	RW	<table><tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Parity selection</td></tr><tr><td>X</td><td>X</td><td>0</td><td>No parity</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Odd parity</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Even parity</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Mark</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Space</td></tr></table> Reset to 000b.
6	Transmission Break	RW	0b: No transmit break condition 1b: Force the transmitter output to a space for alerting the remote receiver of a line break condition. Reset to 0b.
7	Divisor Latch Enable	RW	0b: Data registers are selected 1b: Divisor latch registers are selected Reset to 0b.

7.3.7. MODEM CONTROL REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	DTR Pin Control	RW	0b: Forces DTR output high 1b: Forces DTR output low Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
1	RTS Pin Control	RW	0b: Forces RTS output high 1b: Forces RTS output low Reset to 0b.
2	Output 1	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output1 is routed to RI. Reset to 0b.
3	Output 2	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output2 is routed to DCD. Reset to 0b.
4	Internal Loopback Mode	RW	0b: Disables Internal Loopback Mode 1b: Enables Internal Loopback Mode Reset to 0b.
5	AFE	RW	Autoflow Control Enable. When the AFE is enabled, autoflow control is enabled. When it is disabled, the diagnostic mode is enabled. In the diagnostic mode, transmitted data is immediately received. When AFE is set to "1", MCR Bit 1 is used to enable and disable the auto-RTS. MCR Bit 5 (AFE) / MCR Bit 1 (RTS) / Configuration 1 / 1 / Auto-RTS and auto-CTS are enabled (autoflow control enabled). 1 / 0 / Only auto-CTS is enabled. 0 / x / Auto-RTS and auto-CTS are disabled. Reset to 0b.
6	IrDA Mode	RW	IrDA Mode Enable. 1b: Enables IrDA mode. 0b: Disables IrDA mode. Reset to ENIR pin input.
7	Enhanced Transmission	RW	0b: Insert 1, 1.5 or 2 stop-bits between two transmitted characters. 1b: Insert 0.5 stop-bits between two transmitted characters. Note: Enabling feature may result in certain compatibility issues. This feature is only recommended when using two Pericom UART devices. Reset to 0b.

7.3.8. LINE STATUS REGISTER – OFFSET 05h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	Rx FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	Rx Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
3	Rx Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	Rx Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	Tx Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 0b.
6	Tx Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 0b.
7	Rx Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.3.9. MODEM STATUS REGISTER – OFFSET 06h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Delta CTS	RO	0b: No change in CTS input. 1b: Indicates the CTS input has changed state. This bit is read-clear. Reset to 0b.
1	Delta DSR	RO	0b: No change in DSR input. 1b: Indicates the DSR input has changed state. This bit is read-clear. Reset to 0b.
2	Delta RI	RO	0b: No change in RI input 1b: Indicates the RI input has changed state from the logic 0 to the logic 1. This bit is read-clear. Reset to 0b.
3	Delta DCD	RO	0b: No change in DCD input 1b: Indicates the DCD input has changed state. This bit is read-clear. Reset to 0b.
4	CTS	RO	0b: The CTS input state is the logic 0 1b: The CTS input state is the logic 1 Reset to 0b.
5	DSR	RO	0b: The DSR input state is the logic 0 1b: The DSR input state is the logic 1 Reset to 0b.
6	RI	RO	The input state of RI pin Reset to 0b.
7	DCD	RO	The input state of DCD pin Reset to 0b.

7.3.10. SPECIAL FUNCTION REGISTER – OFFSET 07h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Force Transmission	RW	Forces transmitter to always to transmit data. 1b: Enabled 0b: Disabled Reset to 0b.
1	Auto DSR and DTR Flow Control	RW	Auto DSR and DTR flow control enable 1b: Enables DSR and DTR auto flow control 0b: Disables DSR and DTR auto flow control Reset to 0b.
2	Auto RS-485	RW	Auto RS-485 half-duplex direction control mode enable 1b: Enables RS-485 half-duplex direction control mode 0b: Disables RS-485 half-duplex direction control mode Reset to inversed EN485n pin input.
3	IrDA Invert	RW	Infrared RX input logic select 1b: RX input active LOW (Invert mode) 0b: RX input active HIGH (Normal mode) Reset to 0b.
4	Xon Any Mode	RW	Xon Any mode enable 1b: Enables Xon Any mode 0b: Disables Xon Any mode Reset to 0b.
5	950 Mode	RW	1b: Enables 950 mode 0b: Non-950 mode Reset to 0b.
6	RFD / LSR Counter Select	RW	RFD or LSR counter register select 1b: OFFSET 15 bit[7:0] acts as the Line Status Register Counter 0b: OFFSET 15 bit[7:0] acts as the Receive FIFO Data Counter Reset to 0b.
7	TFD / SCR Select	RW	TFD or SCR register select 1b: OFFSET 16 bit[7:0] acts as the Transmit FIFO Data Counter 0b: OFFSET 16 bit[7:0] acts as the Sample Clock Register Reset to 0b.

7.3.11. DIVISOR LATCH LOW REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor Low	RW	Lower-part of the divisor register Reset to 00h.

7.3.12. DIVISOR LATCH HIGH REGISTER – OFFSET 09h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor High	RW	Higher-part of the divisor register Reset to 00h.

7.3.13. ENHANCED FUNCTION REGISTER – OFFSET 0Ah

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	In-Band Receive Flow Control Mode	RW	When in-band receive flow control is enabled, the UART compares the received data with the programmed XOFF character(s). When this occurs, the UART will disable transmission as soon as any current character transmission is complete. The UART then compares the received data with the programmed XON character(s). When a match occurs, the UART will re-enable transmission (see section 7.11.6). 00b: In-band receive flow control is disabled. 01b: Single character in-band receive flow control enabled, recognising XON2 as the XON character and XOFF2 as the XOFF character. 10b: Single character in-band receive flow control enabled, recognising XON1 as the XON character and XOFF1 and the XOFF character. 11b: The behavior of the receive flow control is dependent on the configuration of EFR[3:2]. Single character in-band receive flow control is enabled, accepting XON1 or XON2 as valid XON characters and XOFF1 or XOFF2 as valid XOFF characters when EFR[3:2] = “01” or “10”. EFR[1:0] should not be set to “11” when EFR[3:2] is ‘00’. Reset to 00b.
3:2	In-Band Transmit Flow Control Mode	RW	When in-band transmit flow control is enabled, XON/XOFF character are inserted into the data stream whenever the RFL passes the upper trigger level and falls below the lower trigger level respectively. For automatic in-band flow control, bit 4 of EFR must be set. The combinations of software transmit flow control can then be selected by programming EFR[3:2] as follows. 00b: In-band transmit flow control is disabled logic. 01b: Single character in-band transmit flow control enabled, using XON2 as the XON character and XOFF2 as the XOFF character. 10b: Single character in-band transmit flow control enabled, using XON1 as the XON character and XOFF1 as the XOFF character. 11b: The value EFR[3:2] = “11” is reserved for future use and should not be used Reset to 00b.
4	Enhanced Mode	RW	0b: Non-Enhanced mode. 1b: Enhanced mode. Enables the Enhanced Mode functions. If use addition function except 16550 mode. Reset to 0b.
5	Special Character Detection Enable	RW	0b: Special character detection is disabled. 1b: While in Enhanced mode (EFR[4]=1), the UART compares the incoming receiver data with the XOFF1 or XOFF2 value and interrupt will be asserted. If In-Band Flow Control is enabled, this bit must be set to ‘1’. Reset to 0b.
6	Automatic RTS Flow Control Enable	RW	0b: RTS flow control is disabled. 1b: RTS flow control is enabled in Enhanced mode (i.e. EFR[4] = 1), where the RTS# pin will be forced inactive high if the RFL reaches the upper flow control threshold. This will be released when the RFL drops below the lower threshold. 650 and 950-mode drivers should use different threshold level. Reset to 0b.
7	Automatic CTS Flow Control	RW	0b: CTS flow control is disabled (default). 1b: CTS flow control is enabled in Enhanced mode (i.e. EFR[4]

BIT	FUNCTION	TYPE	DESCRIPTION
	Enable		= 1), where the data transmission is prevented whenever the CTS# pin is held inactive high. 650 and 950-mode drivers should use different threshold level. Reset to 0b.

7.3.14. XON SPECIAL CHARACTER 1 – OFFSET 0Bh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XON1	RW	Xon character 1. Reset to 00h.

7.3.15. XON SPECIAL CHARACTER 2 – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XON2	RW	Xon character 2. Reset to 00h.

7.3.16. XOFF SPECIAL CHARACTER 1 – OFFSET 0Dh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XOFF1	RW	Xoff character 1. Reset to 00h.

7.3.17. XOFF SPECIAL CHARACTER 2 – OFFSET 0Eh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XOFF2	RW	Xoff character 2. Reset to 00h.

7.3.18. ADVANCE CONTROL REGISTER – OFFSET 0Fh

BIT	FUNCTION	TYPE	DESCRIPTION
0	Transmitter Terminate Condition	RO	Indicates current transmitter terminate condition. If transmitter is disabled by remote terminate, the condition can be shown by this bit. 1b: Disabled by remote terminate. 0b: The transmitter can transmit data normally. Reset to 0b.
1	Remote TX Disable	RO	Remote TX Disable. 1b: If transmitter has sent XOFF message or RTS message, then DTR is inactive, and then it is enabled. 0b: otherwise Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
2	Xon/Xoff Detect	RO	When receiving a XON/XOFF character from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. If the Xoff/Special Character Interrupt is enabled, the Xoff Detect status is also reflected in the Interrupt Status Register (Priority Level 6). 1b: Event true 0b: Event false Reset to 0b.
3	Special Character Detect	RO	When detecting the special characters from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. If the Xoff/Special Character Interrupt is enabled, the status is also reflected in the Interrupt Status Register (Priority Level 6). 1b: Event true 0b: Event false Reset to 0b.
4	Xon Detect	RO	When receiving a XON character from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. 1b: Event true 0b: Event false Reset to 0b.
5	Xoff Detect	RO	When receiving a XOFF character from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. 1b: Event true 0b: Event false Reset to 0b.
7:6	Reserved	RO	Reset to 00b.

7.3.19. TRANSMIT INTERRUPT TRIGGER LEVEL – OFFSET 10h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TTL	RW	Transmitter Interrupt Trigger Level. Reset to 00h.

7.3.20. RECEIVE INTERRUPT TRIGGER LEVEL – OFFSET 11h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	RTL	RW	Receiver Interrupt Trigger Level. Reset to 00h.

7.3.21. FLOW CONTROL LOW TRIGGER LEVEL – OFFSET 12h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FCL	RW	Automatic Flow Control Low Trigger Level. Reset to 00h.

7.3.22. FLOW CONTROL HIGH TRIGGER LEVEL – OFFSET 13h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FCH	RW	Automatic Flow Control High Trigger Level. Reset to 00h.

7.3.23. CLOCK PRESCALE REGISTER – OFFSET 14h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	CPRN	RW	N number in calculating the Prescaler, which is used to generate the Baud Rate. Reset to 000b.
7:3	CPRM	RW	M number in calculating the Prescaler, which is used to generate the Baud Rate. It is recommended that the value of the CPRM be set to “00001” or “00010”. Reset to 00001b.

7.3.24. RECEIVE FIFO DATA COUNTER – OFFSET 15h, SFR[6] = 0

The function of this register is selected by the Special Function Register (Offset 07h) bit 6. When SFR[6] is set to ‘1’, this register functions as the Receive FIFO Data Counter. Otherwise, it functions as the Line Status Register Counter.

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Receive FIFO Data Counter	RO	The Receive FIFO Data Counter indicates the amount of data in the Receive FIFO. Reset to 00h.

7.3.25. LINE STATUS REGISTER COUNTER – OFFSET 15h, SFR[6] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Line Status Register Counter	RO	The Line Status Register Counter indicates the amount of data in the LSR. Reset to 00h.

7.3.26. TRANSMIT FIFO DATA COUNTER – OFFSET 16h, SFR[7] = 1

The function of this register is selected by the Special Function Register (Offset 07h) bit 7. When SFR[7] is set to ‘1’, this register functions as the Transmit FIFO Data Counter. Otherwise, it functions as the Sample Clock Register.

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Transmit FIFO Data Counter	RO	The Transmit FIFO Data Counter indicates the amount of data in the Transmit FIFO. Reset to 00h.

7.3.27. SAMPLE CLOCK REGISTER – OFFSET 16h, SFR[7] = 0

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Sample Clock	RW	This register determines the Sample Clock value (SC) used in the Baud Rate Generator. Please refer to 5.2.12 Baud Rate Generation for more detail 0000b: SC = 16 0001b: SC = 15 0010b: SC = 14 0011b: SC = 13 0100b: SC = 12 0101b: SC = 11 0110b: SC = 10 0111b: SC = 9 1000b: SC = 8 1001b: SC = 7 1010b: SC = 6 1011b: SC = 5 1100b: SC = 4 Other settings are reserved. Reset to 0h.
7:4	Reserved	RO	Reset to 0h.

7.3.28. GLOBAL LINE STATUS REGISTER – OFFSET 17h

BIT	FUNCTION	TYPE	DESCRIPTION
0	RX Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	RX FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	RX Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.
3	RX Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	RX Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	TX Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 0b.
6	TX Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 0b.
7	RX Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.3.29. GLOBAL INTERRUPT ENABLE REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enable Channel 0-7 Interrupt	RW	1b: INT enable Reset to FFh.

7.3.30. GLOBAL INTERRUPT STATUS REGISTER – OFFSET 19h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Channel 0-7 Interrupt Status	RO	1b: INT is pending Reset to 00h

7.3.31. TX OVERRUN REGISTER – OFFSET 1Ah

BIT	FUNCTION	TYPE	DESCRIPTION
6:0	Reserved	RO	Reset to 00h
7	TX Overrun Index	RO	This bit set indicates TX has ever overrun Reset to 0b

7.3.32. RX OVERRUN REGISTER – OFFSET 1Bh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0h
4	TX Overrun Index	RO	This bit set indicates RX has ever overrun Reset to 0b
7:5	Reserved	RO	Reset to 000b

7.3.33. INTERRUPT STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RO	 Reset to 0b.
1	RX Error Interrupt	RO	0b: No RX error interrupt pending 1b: RX error interrupt pending Reset to 0b.
2	RX Ready Interrupt	RO	0b: No RX ready interrupt pending 1b: RX ready interrupt pending Reset to 0b.
3	RX Timeout Interrupt	RO	0b: No RX timeout interrupt pending 1b: RX timeout interrupt pending Reset to 0b.
4	THR Empty Interrupt	RO	0b: No THR empty interrupt pending 1b: THR empty interrupt pending Reset to 0b.
5	Modem Interrupt	RO	0b: No Modem interrupt pending 1b: Modem interrupt pending Reset to 0b.
6	Xoff Interrupt	RO	0b: No Xoff interrupt pending 1b: Xoff interrupt pending Reset to 0b.
7	RTS/CTS Interrupt	RO	0b: No RTS/CTS interrupt pending 1b: RTS/CTS interrupt pending Reset to 0b.

7.3.34. RX FIFO COUNTER – OFFSET 1Dh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	RX FIFO Counter	RO	RX FIFO Counter Reset to 00h

7.3.35. TX FIFO COUNTER – OFFSET 1Eh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TX FIFO Counter	RO	TX FIFO Counter Reset to 00h

7.3.36. FCR MIRROR REGISTER – OFFSET 1Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Mirror of FCR set	RO	Read of the FCR register setting Reset to 00h

7.3.37. USER DEFINED TIMEOUT COUNTER REGISTER-1 – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TIMEOUT_REG[7:0]	RW	User defined timeout counter register LSB Reset to 00h

7.3.38. USER DEFINED TIMEOUT COUNTER REGISTER-2 – OFFSET 21h

BIT	FUNCTION	TYPE	DESCRIPTION
6:0 7	TIMEOUT_REG[14:8] Reserved	RW RO	User defined timeout counter register MSB Reset to 00h

7.3.39. USER DEFINED TRIGGER LEVEL REGISTER – OFFSET 22h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	RXTH_REG[7:0]	RW	User defined trigger level Reset to 00h

7.3.40. USER DEFINED REGISTER ENABLE – OFFSET 23h

BIT	FUNCTION	TYPE	DESCRIPTION
0 1 7:2	TIMEOUT_EN_REG RXTH_EN_REG Reserved	RW RW	User defined timeout register enable User defined trigger level register enable Reset to 00h

7.3.41. TX IDLE COUNTER REGISTER– OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TX Idle Counter	RW	User defined TX idle counter Reset to 00h

7.3.42. TX IDLE ENABLE REGISTER– OFFSET 25h

BIT	FUNCTION	TYPE	DESCRIPTION
0	TX Idle Enable	RW	1b: Enable TX idle Reset to 1b
1	RX Timeout Enable	RW	1b: Enable RX timeout Reset to 1b
6:2	Reserved	RO	Reset to 00h

7.3.43. SPECIAL CHARACTER 1 REGISTER– OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SPCH1	RW	The number 1 special character register Reset to 00h

7.3.44. SPECIAL CHARACTER 2 REGISTER– OFFSET 29h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SPCH2	RW	The number 2 special character register Reset to 00h

7.3.45. SPECIAL CHARACTER 3 REGISTER– OFFSET 2Ah

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SPCH3	RW	The number 3 special character register Reset to 00h

7.3.46. SPECIAL CHARACTER 4 REGISTER– OFFSET 2Bh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SPCH4	RW	The number 4 special character register Reset to 00h

7.3.47. SPECIAL CHARACTER ENABLE / CLEAR REGISTER– OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0 7:4	SPCH_EN SPCH_CLR	RW RW	Enable special character register 1-4 Clear special character register 1-4 Reset to 00h

7.3.48. FLASH LSR/TX_EMPTY INTERRUPT REGISTER– OFFSET 2Dh

BIT	FUNCTION	TYPE	DESCRIPTION
0	TX_EMPTY_EN	RW	When set, TX FIFO empty interrupt is enabled Reset to 1b
1	FLASH_LSR_EN	RW	When set, LSR FIFO is read following the DATA FIFO reading Reset to 1b
7:2	Reserved	RO	Reset to 00h

7.3.49. IN BAND TRANSMIT FLOW CONTROL REGISTER– OFFSET 2Eh

BIT	FUNCTION	TYPE	DESCRIPTION
0	IN BAND CTL	RW	When set, In band transmit turn off to enable send XON Reset to 1b
7:1	Reserved	RO	Reset to 00h

7.3.50. ADVANCE CONTROL REGISTER– OFFSET 2Fh

BIT	FUNCTION	TYPE	DESCRIPTION
0	RX Disable	RW	When set, receiver be disabled Reset to 0b
1	TX Disable	RW	When set, transmitter be disabled Reset to 0b
3:2	Reserved	RO	Reset to 00b
4	IrDA 1.1	RW	IrDA 1.1 fast mode enable when set Reset to 0b
5	RS-485 CTL	RW	Auto RS-485 direction control polarity inversion: 0b: RTS# output is LOW when transmitting and HIGH when receiving 1b: RTS# output is HIGH when transmitting and LOW when receiving Reset to 0b
6	RS-485 9-bit	RW	When set, enable RS-485 9-bit mode Reset to 0b
7	Reserved	RO	Reset to 0b

7.3.51. RECEIVE FIFO DATA REGISTERS – OFFSET 100h ~ 17Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Receive FIFO Data	RO	This register is used to map RX FIFO data content. Reset to 00h.

7.3.52. TRANSMIT FIFO DATA REGISTERS – OFFSET 100h ~ 17Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Transmit FIFO Data	WO	This register is used to map TX FIFO to memory space. Reset to 00h.

7.3.53. LINE STATUS FIFO REGISTERS –OFFSET 180h ~ 1FFh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Line Status FIFO	RO	This register is used to map FIFO data relative LSR content. Reset to 00h.

The Device Configuration Registers Accessible Channle-0 Only

7.3.54. GLOBAL INTERRUPT REGISTERS 0 –OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	This register shows individual interrupt status for each channel Reset to 00h.

INT0[7]	INT0[6]	INT0[5]	INT0[4]	INT0[3]	INT0[2]	INT0[1]	INT0[0]
Reserved	Reserved	Reserved	Reserved	CH-3	CH-2	CH-1	CH-0

7.3.55. GLOBAL INTERRUPT REGISTERS 1 –OFFSET 41h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	This register shows encoded interrupt indicator (3-bits per channel) Reset to 00h.

7.3.56. GLOBAL INTERRUPT REGISTERS 2 –OFFSET 42h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	This register shows encoded interrupt indicator (3-bits per channel) Reset to 00h.

7.3.57. GLOBAL INTERRUPT REGISTERS 3 –OFFSET 43h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	This register shows encoded interrupt indicator (3-bits per channel) Reset to 00h.

INT1[7]	INT1[6]	INT1[5]	INT1[4]	INT1[3]	INT1[2]	INT1[1]	INT1[0]
CH-2[1]	CH-2[0]	CH-1[2]	CH-1[1]	CH-1[0]	CH-0[2]	CH-0[1]	CH-0[0]
INT2[7]	INT2[6]	INT2[5]	INT2[4]	INT2[3]	INT2[2]	INT2[1]	INT2[0]
Reserved	Reserved	Reserved	Reserved	CH-3[2]	CH-3[1]	CH-3[0]	CH-2[2]
INT3[7]	INT3[6]	INT3[5]	INT3[4]	INT3[3]	INT3[2]	INT3[1]	INT3[0]
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Priority	Bit[2]	Bit[1]	Bit[0]	Interrupt Source And Clearing
X	0	0	0	None or wake-up indicator
1	0	0	1	RX line status
2	0	1	0	RX time-out
3	0	1	1	THR or TSR empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR Delta, Xoff/Xon or Special Character detected
5	1	0	1	Reserved
6	1	1	0	GPIO pin(s), shows up on channel_0 only
7	1	1	1	TIMER time-out, shows up on channel_0 only

7.3.58. TIMER CONTROL REGISTER –OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Interrupt Enable	RW	Enable timer interrupt 1b: Enables timer interrupt 0b: Disables timer interrupt Reset to 0b.
1	Start Timer	RW	Timer start when set Reset to 0b.
2	Function Select	RW	Timer control function select Reset to 0b.
3	Clock Source	RW	Select Clock Source Reset to 0b.
7:4	Reserved	RO	Reset to 0h.

TIMER_CTL[3:0]	Timer Control Commands Decode
0001	Enable timer interrupt
0010	Disable timer interrupt
0011	Select one-shot mode
0100	Select re-trigger mode
0101	Select internal clock source for the timer
0110	Select external clock source for the timer
0111	Reserved
1000	Reserved
1001	Start timer
1010	Stop timer
1011	Reset timer
1100-1111	Reserved

7.3.59. TIMER/COUNTER LATCH LSB REGISTER –OFFSET 46h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Timer/Counter LSB	RW	LSB bits of timer/counter Reset to 00h.

7.3.60. TIMER/COUNTER LATCH MSB REGISTER –OFFSET 47h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Timer/Counter MSB	RW	MSB bits of timer/counter Reset to 00h.

7.3.61. SOFTWARE RESET REGISTER –OFFSET 4Ah

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	UART Reset	WOS	Individual UART channel reset enable. 1b: UART reset 0b: Normal Reset to 00h.

7.3.62. SLEEP MODE CONTROL REGISTER –OFFSET 4Bh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	UART Reset	RW	Individual enable UART channel sleep mode. 1b: UART channel sleep mode enable 0b: Disables UART channel sleep mode Reset to 00h.

7.3.63. DEVICE REVISION REGISTER –OFFSET 4Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Device Revision	RO	Revision number of PI7C8954 Reset to 01h.

7.3.64. DEVICE IDENTIFICATION REGISTER –OFFSET 4Dh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Device ID	RO	The device ID for PI7C8954 Reset to 58h.

7.3.65. SIMULTANEOUS CONFIGURATION ALL UART REGISTER –OFFSET 4Eh

BIT	FUNCTION	TYPE	DESCRIPTION
0	Simultaneous Configuration All UART	RW	When set, enable write to all UART channels Reset to 0b.
7:1	Reserved	RO	Reset to 00h

7.3.66. GENERALPURPOSE IO INTERRUPT MASK REGISTER –OFFSET 4Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO Interrupt Mask	RW	When set, the input status change interrupt enable Reset to 00h.

7.3.67. GENERALPURPOSE IO OUTPUT LEVEL CONTROL REGISTER –OFFSET 50h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO Output Level Control	RW	GPIO output level control: 0b: output LOW 1b: output HIGH Reset to 00h.

7.3.68. GENERALPURPOSE IO OUTPUT STATE CONTROL REGISTER –OFFSET 51h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO Output State Control	RW	GPIO output state control: 0b: output normal 1b: tri-state Reset to 00h.

7.3.69. GENERALPURPOSE IO INPUT POLARITY SELECT REGISTER –OFFSET 52h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO Input Polarity	RW	Select GPIO input polarity: 0b: input normal 1b: invert the input in logic Reset to 00h.

7.3.70. GENERALPURPOSE IO SELECT REGISTER –OFFSET 53h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO In/Out Select	RW	Select GPIO pin IN/OUT direction: 0b: input 1b: output Reset to 00h.

8. EEPROM INTERFACE

An external 93C46 EEPROM is only used to store the vendor's ID and model number, and the sub-vendor's ID and product model number. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, if your design requires non-volatile memory for other purpose, it is possible to store and retrieve data on the EEPROM through a special PCI device configuration register.

8.1. EEPROM MODE AT RESET

During a reset, the device will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the auto load initiates right after the reset.

8.2. EEPROM SPACE ADDRESS MAP AND DESCRIPTION

EEPROM ADDRESS	PCI REGISTER OFFSET	DEFAULT Value	DESCRIPTION
00h		A868h	**Check Code**
02h	Offset 00h bit[15:0]	12D8h	**Vendor ID**
04h	Offset 00h bit[31:16]	8954h	**Device ID**
06h	Offset 2Ch bit[15:0]	0000h	**Subsytem Vendor ID**
08h	Offset 2Ch bit[31:16]	0000h	**Subsytem ID**
0Ah	Offset 08h bit[7:0]	00h	**Revision ID**
0Ch		FFFFh	**Stop Code**

9. ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Power Supply Range (VCC&VIO)	7 volts
Voltage at any Signal Pin	-0.5 to 7 volts
Storage Temperature	-65° to +150° C

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 1.62-5.5V)

TA= -40 ° to +85°C

Symbol	Parameter	Min	Max	Units	Condition	Notes
V_{IL}	Input Low Voltage	-0.5	0.8	V		All inputs
V_{IH}	Input High Voltage	2.0	VIO + 0.5	V		PCI bus and External Clock inputs
V_{IH}	Input High Voltage	1.6	6.0	V		Non-PCI bus inputs
V_{OL}	Output Low Voltage		0.55	V	Iout=6 mA	All outputs
V_{OH}	Output High Voltage	2.4		V	Iout=-2 mA	All outputs
I_{IL}	Input Low Leakage Current		-10	uA		
I_{IH}	Input High Leakage Current		10	uA		
I_{CL}	Input Clock Leakage		±10	uA		
C_{IN}	Input Pin Capacitance		10	pF		
C_{CLK}	CLK Pin Capacitance	5	12	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8	pF		
I_{CC}	Power Supply Current		10	mA	PCI Bus CLK and Ext. Clock=2MHz, all inputs are at VCC or GND and all outputs are unloaded	
I_{SLEEP}	Sleep Current		800	uA	All UARTs asleep. AD[31:0] at GND, all inputs at VCC or GND.	

AC ELECTRICAL CHARACTERISTICS FOR 5V PCI BUS INTERFACE (VIO = 4.75-5.25V, VCC = 1.62-5.5V)

TA=0° to 70°C (-40° to +85°C for industrial grade package).

Symbol	Parameter	Min	Max	Units	Notes
XTAL1	UART Crystal Oscillator		24	MHz	
ECLK	External Clock		80	MHz	VCC=3.3V ±10%
T_{ECLK}	External Clock Period	12		ns	T_{ECLK} = 1/ECLK
T_{ECH}, T_{ECL}	External Clock High/Low Time	5		ns	
$I_{OH(AC)}$	Switching Current High	-44		mA	See PCI Specification Rev. 2.3
$I_{OL(AC)}$	Switching Current Low	95		mA	See PCI Specification Rev. 2.3
I_{CL}	Low Clamp Current	-25+(Vin+1)/0.015		mA	-5 < Vin ≤ -1
$Slew_R$	Output Rise Slew Rate	1	4	V/ns	0.4V to 2.4V load
$Slew_F$	Output Fall Slew Rate	1	4	V/ns	2.4V to 0.4V load
T_{CYC}	CLK Cycle Time	15	∞	ns	PCI Bus Clock, CLK
T_{HI}	CLK High Time	6		ns	
T_{LO}	CLK Low Time	6		ns	
	CLK Slew Rate	1.5	4	V/ns	
T_{VAL}	CLK to Signal Valid Delay	2	6	ns	
T_{ON}	Float to Active Delay	2		ns	
T_{OFF}	Active to Float Delay		12	ns	
T_{SETUP}	Input Setup Time to CLK - bused signals	3		ns	
T_{HOLD}	Input Hold Time from CLK	0		ns	
T_{PRST}	RST# Active Time After Power Stable	1		ms	
$T_{CRST\#}$	RST# Active Time After CLK Stable	100		us	
	RST# Slew Rate	50		mV/ns	

DC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 3.0-5.5V)

TA= -40 ° to +85°C

Symbol	Parameter	Min	Max	Units	Condition	Notes
V_{IL}	Input Low Voltage	-0.5	0.3VIO	V		For PCI bus inputs
V_{IL}	Input Low Voltage	-0.5	0.8	V		For Non-PCI bus inputs

DC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 1.62-5.5V)

TA= -40° to +85°C

Symbol	Parameter	Min	Max	Units	Condition	Notes
V_{IH}	Input High Voltage	0.5VIO	VIO + 0.5			For PCI bus and external clock inputs
V_{IH}	Input High Voltage	1.6	6	V		For non-PCI bus inputs
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4mA	All outputs
V_{OH}	Output High Voltage	0.9VIO		V	I_{OH} = -0.5mA	PCI bus outputs
V_{OH}	Output High Voltage	2.0		V	I_{OH} = -1mA VCC = 3.0 - 3.6V	Non-PCI bus outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2mA VCC = 4.5 - 5.5V	Non-PCI bus outputs
I_{IL}	Input Low Leakage Current		-10	µA		
I_{IH}	Input High Leakage Current		10	µA		
I_{CL}	Input Clock Leakage		±10	µA		
C_{IN}	Input Pin Capacitance		10	pF		
C_{CLK}	CLK Pin Capacitance	5	12	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8	pF		
I_{CC}	Power Supply Current		10	mA	PCI Bus CLK and Ext. Clock=2MHz, all inputs are at VCC or GND and all outputs are unloaded	
I_{SLEEP}	Sleep Current		800	µA	All UARTs asleep. AD[31:0] at GND, all inputs at VCC or GND	

AC ELECTRICAL CHARACTERISTICS FOR 3.3V PCI BUS INTERFACE (VIO = 3.0-3.6V, VCC = 1.62-5.5V)

TA= -40° to +85°C

Symbol	Parameter	Min	Max	Units	Notes
XTAL1	UART Crystal Oscillator		24	MHz	On-chip osc.
ECLK	External Clock		80	MHz	VCC = 3.3V ±10%
T_{ECLK}	External Clock Period (T_{ECLK} = 1/ECLK)	12		ns	VCC = 3.3V ±10%
T_{ECH}, T_{ECL}	External Clock High/Low Time	5		ns	VCC = 3.3V ±10%
$I_{OH(AC)}$	Switching Current High	-12VIO		mA	See PCI Specification Rev. 2.3
$I_{OL(AC)}$	Switching Current Low	16VIO		mA	See PCI Specification Rev. 2.3
I_{CH}	High Clamp Current	25+(Vin-VIO-1)/0.015		mA	VIO+4 > Vin ≥ VIO+1
I_{CL}	Low Clamp Current	-25+(Vin+1)/0.015		mA	-3 < Vin ≤ -1
$Slew_R$	Output Rise Slew Rate	1.5	4	V/ns	0.2VIO - 0.6VIO load
$Slew_F$	Output Fall Slew Rate	1.5	4	V/ns	0.6VIO - 0.2VIO load
T_{CYC}	CLK Cycle Time	15	∞	ns	PCI Bus Clock, CLK
T_{HI}	CLK High Time	6		ns	
T_{LO}	CLK Low Time	6		ns	
	CLK Slew Rate	1.5	4	V/ns	
T_{VAL}	CLK to Signal Valid Delay	2	6	ns	
T_{ON}	Float to Active Delay	2		ns	
T_{OFF}	Active to Float Delay		12	ns	
T_{SETUP}	Input Setup Time to CLK - bused signals	3		ns	
T_{HOLD}	Input Hold Time from CLK	0		ns	
T_{PRST}	RST# Active Time After Power Stable	1		ms	
$T_{CRST\#}$	RST# Active Time After CLK Stable	100		us	
	RST# Slew Rate	50		mV/ns	

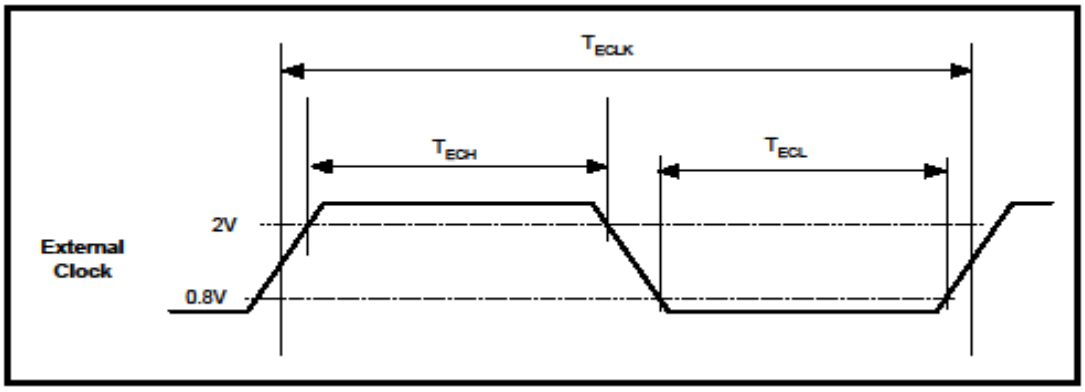


Figure 9-1 Timing For External Clock Input at XTAL1 Pin

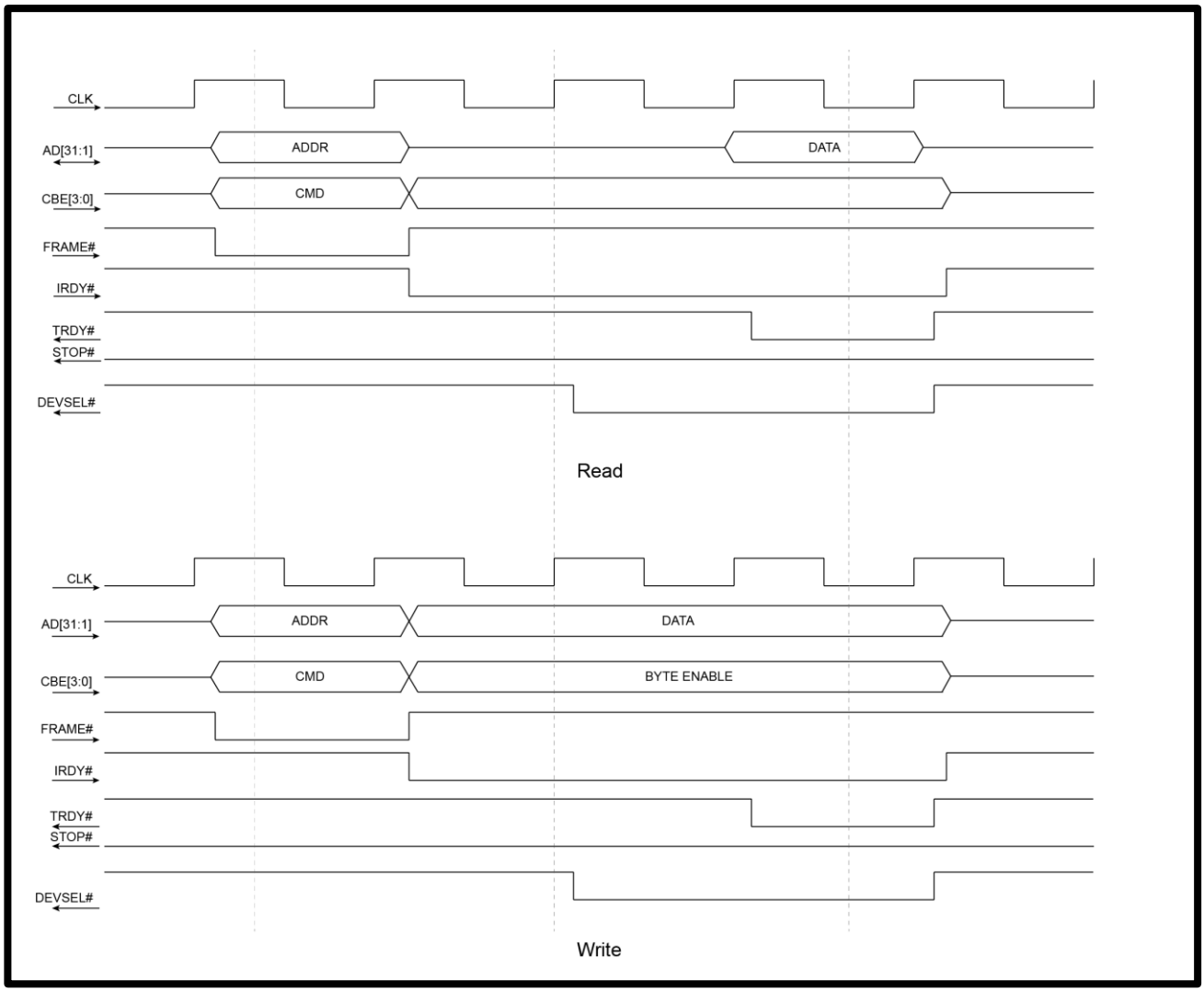


Figure 9-2 PCI Bus Configuration Space and UART Registers Read and Write Operation

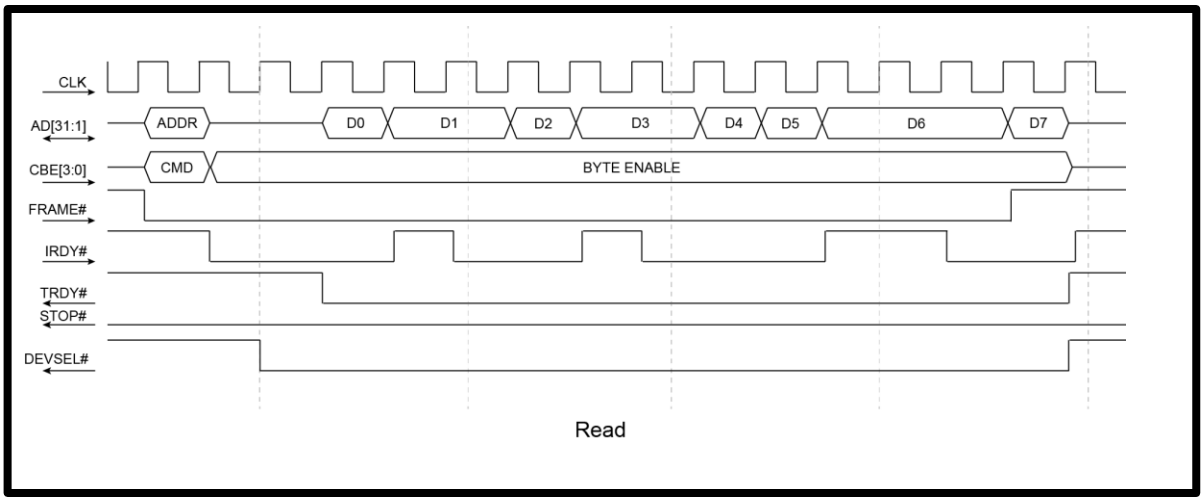


Figure 9-3 Receive data burst read operation

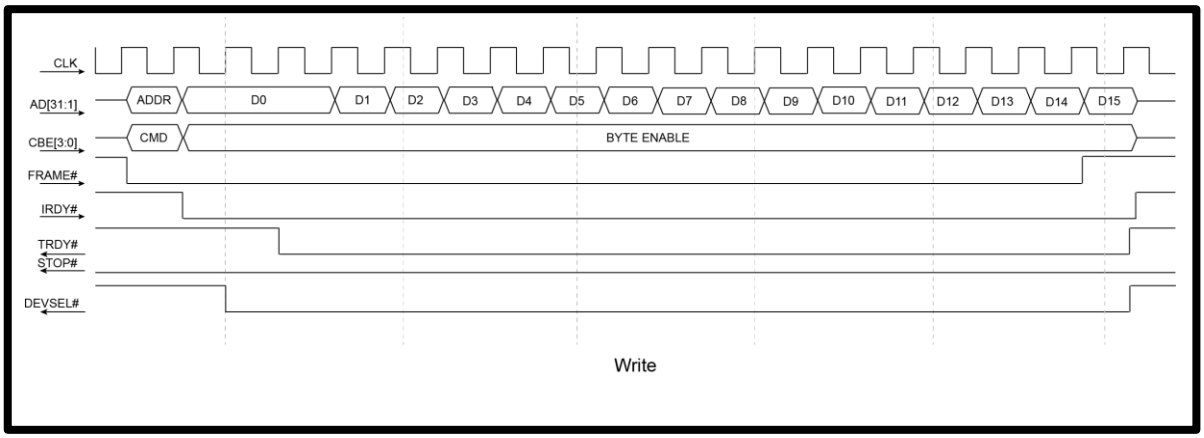


Figure 9-4 Transmit data burst write operation

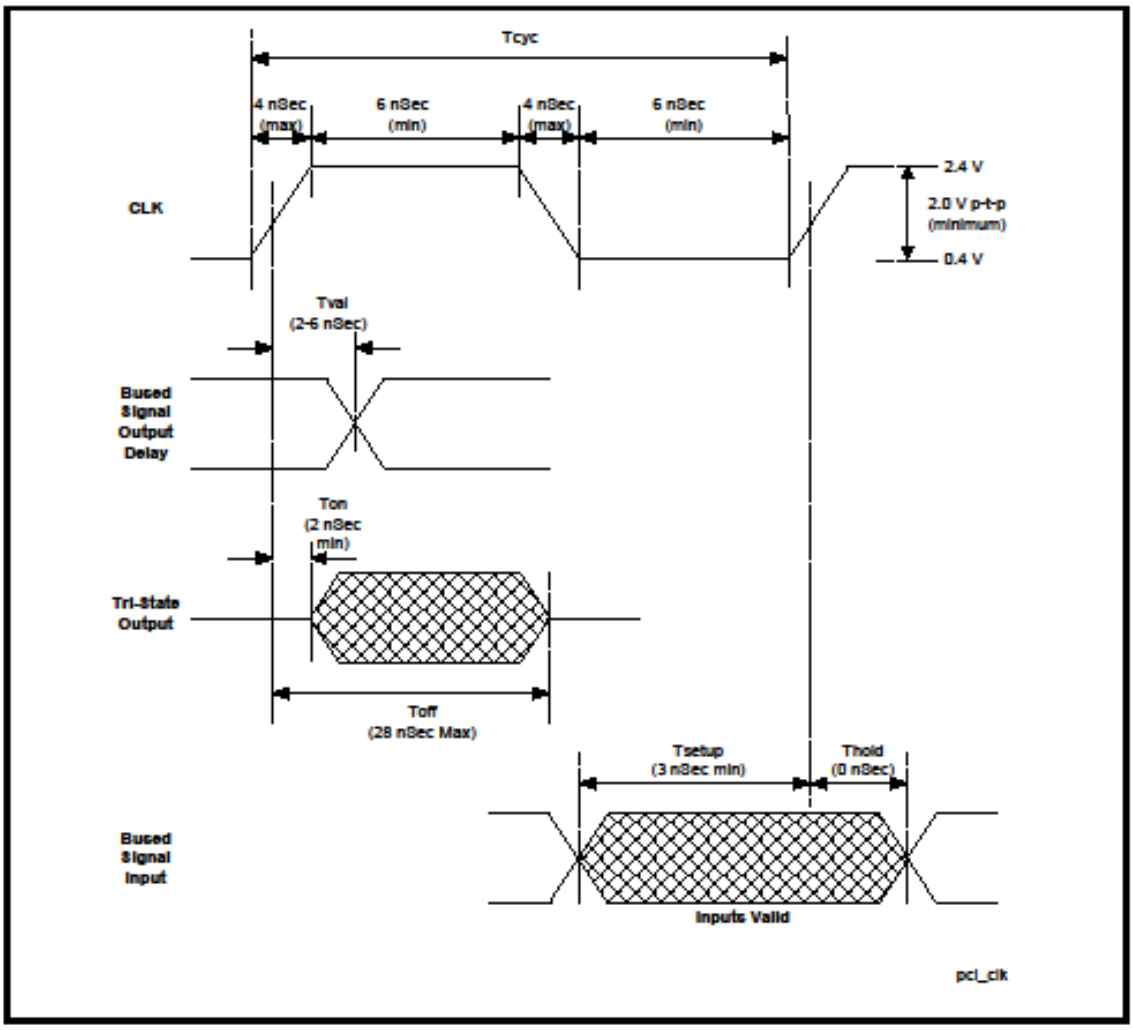


Figure 9-5 5V PCI Bus Clock (DC to 66MHz)

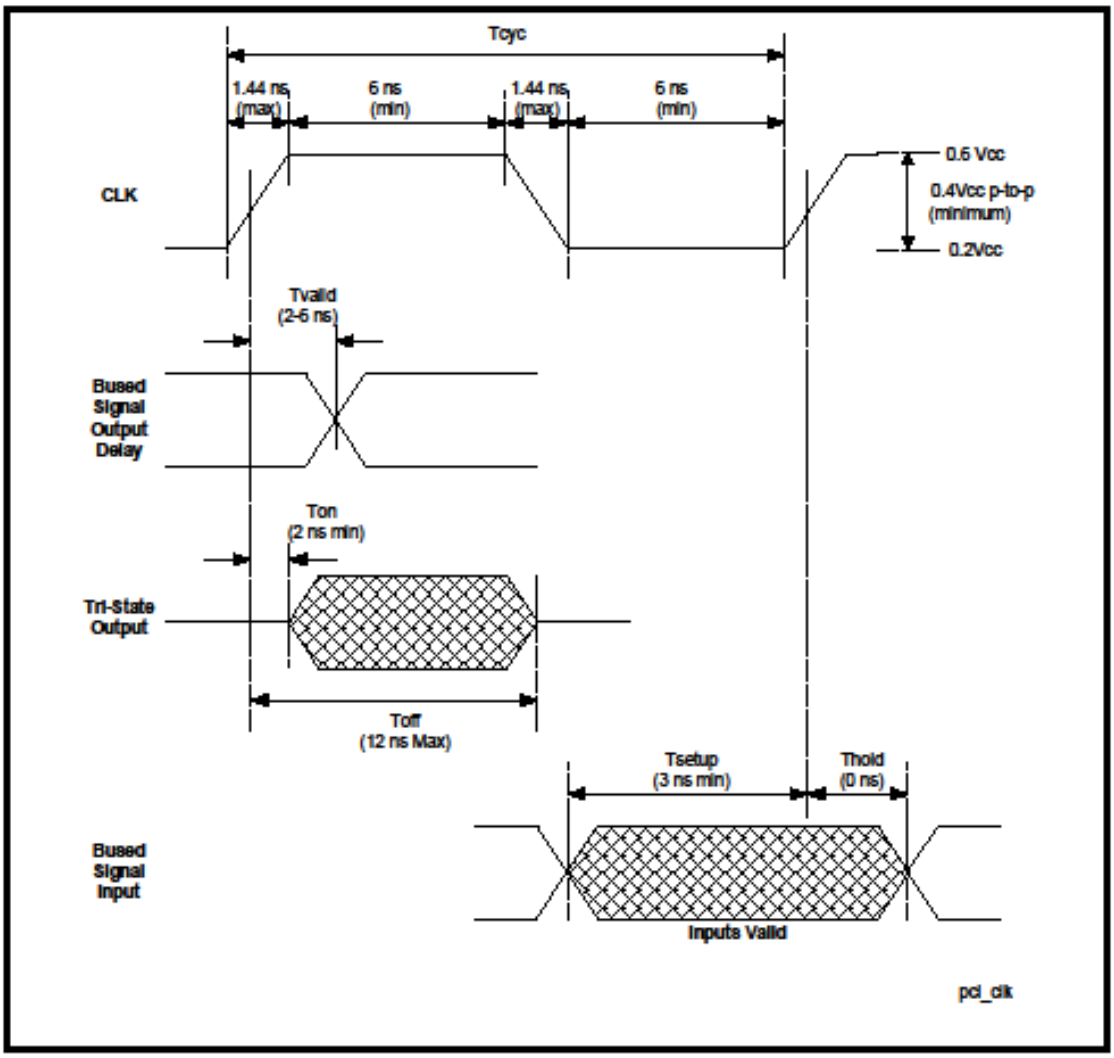


Figure 9-6 3.3V PCI Bus Clock (DC to 66MHz)

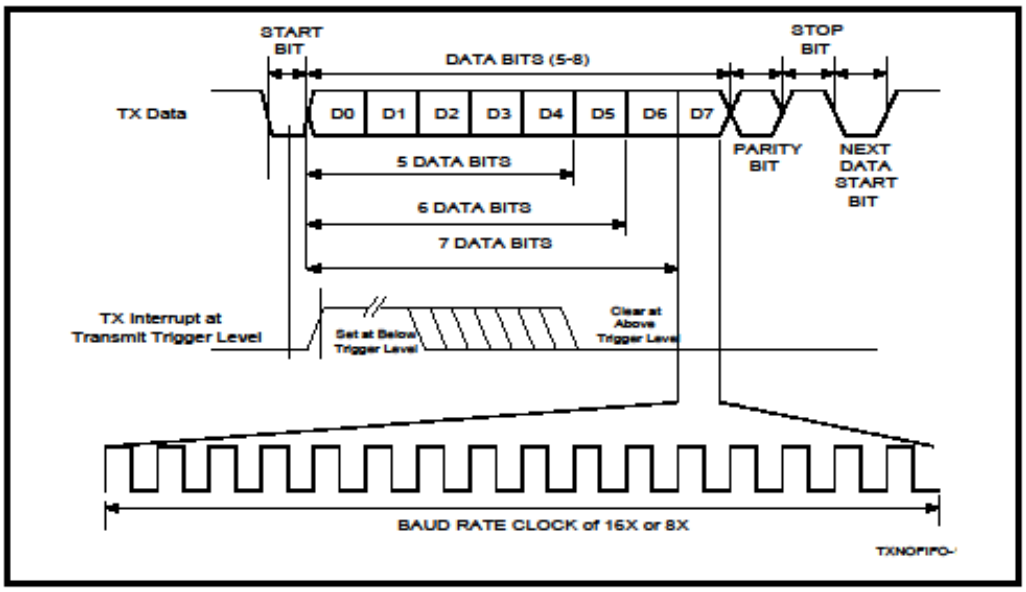


Figure 9-7 Transmit Data Interrupt at Trigger Level

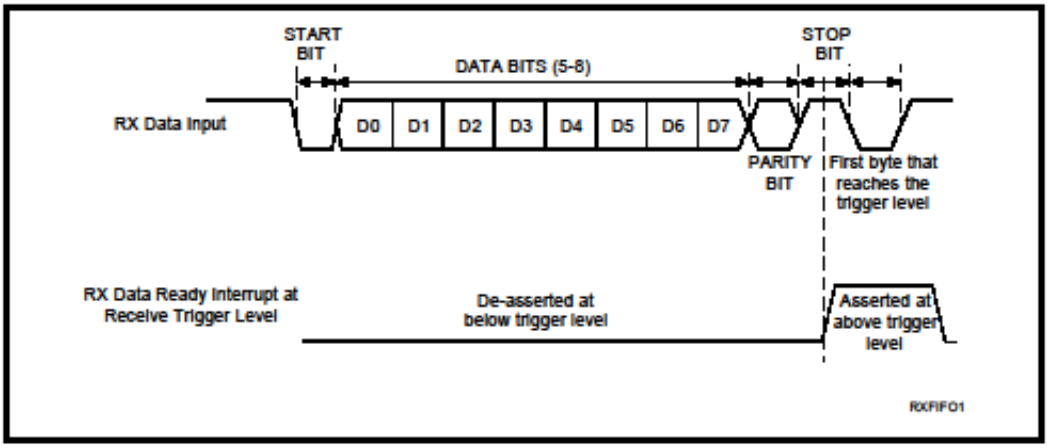
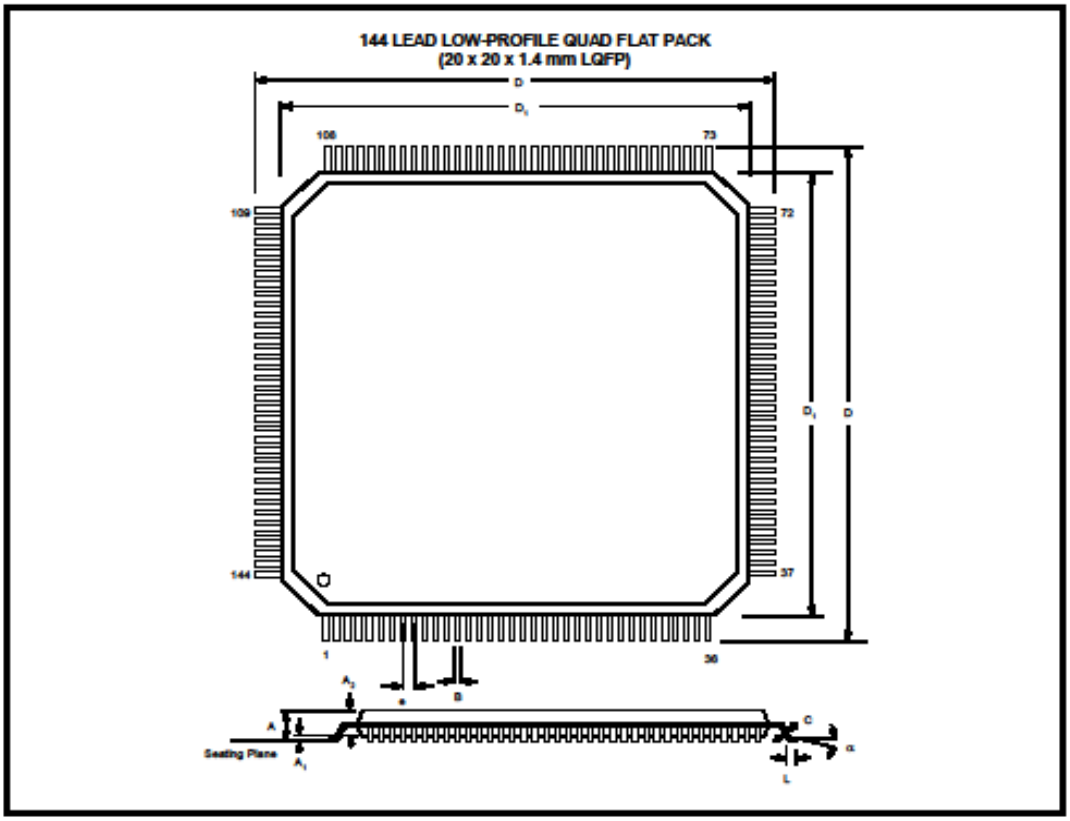


Figure 9-8 Receive Data Ready Interrupt at Trigger Level

10. PACKAGE INFORMATION

The Package of the PI7C8954 is a 144-pin LQFP. The following are the package information and mechanical dimensions.

PACKAGE DIMENSIONS



Note: Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D1	0.783	0.791	19.90	20.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Figure 10-1 Package outline drawing

11. Order Information

Part Number	Temperature Range	Package	Pb-Free & Green
PI7C8954□FHEX	-40° to 85°C (Industrial Temperature)	144-pin LQFP 20mm x 20mm	Yes