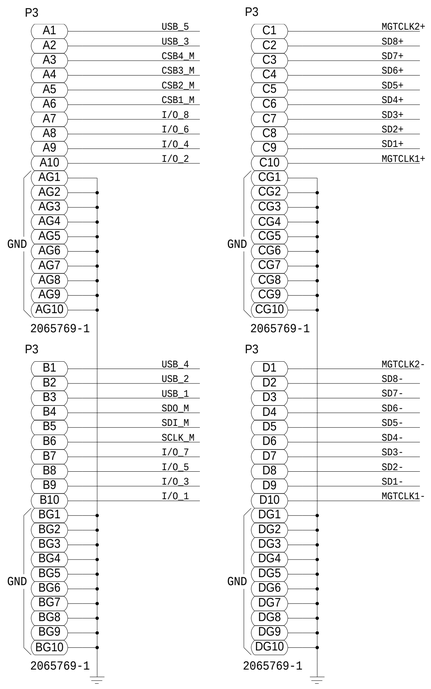
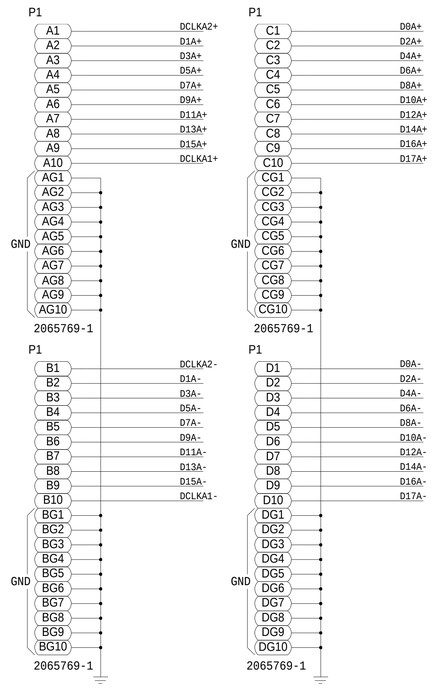
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

EVAL BOARD CONNECTIONS

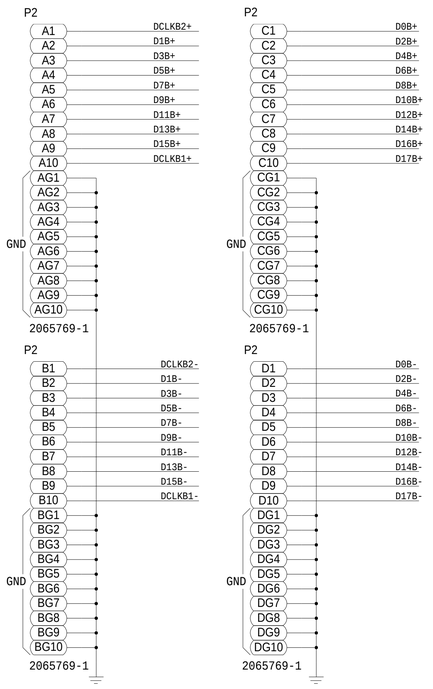
(J1) HS-SERIAL/SPI/AUX

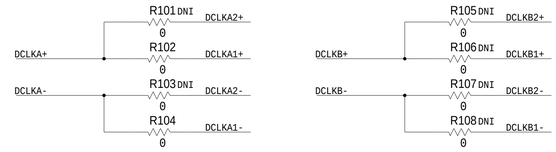


(J3) DATA BUS 2



(J2) DATA BUS 1





SELECT GLOBAL CLOCK OR CLOCK CAPABLE IO

ANALOG DEVICES

SCHEMATIC

<DRAWING_TITLE_HEADER>
CVTADCFMCINTPZ
ENGINEERING BOARD

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. CVTADCFMCINTPZ01		REV B
PTD ENGINEER R. Reeder	SIZE D	SCALE NONE	SHEET 1 OF 2

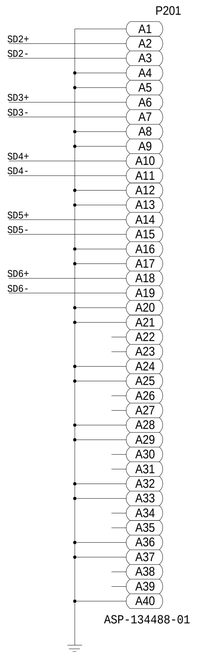
FMC CONNECTIONS

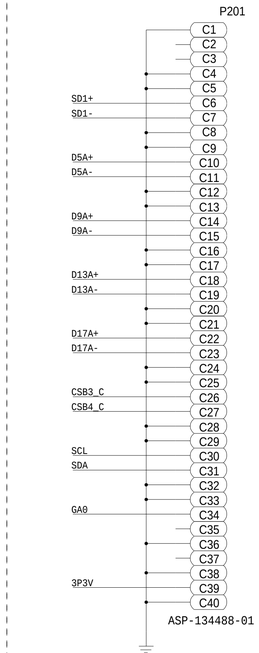
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

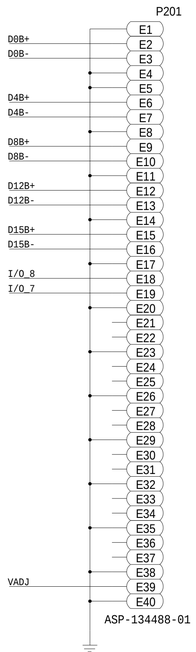
NOTE:

3P3V = 3.3V
VADJ = 3.3V - 0V

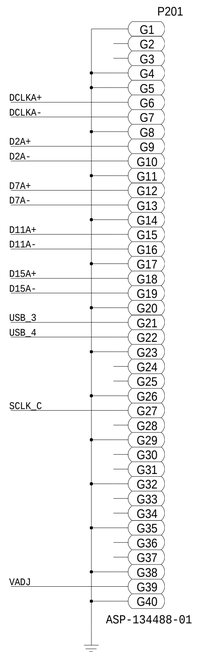
LPC

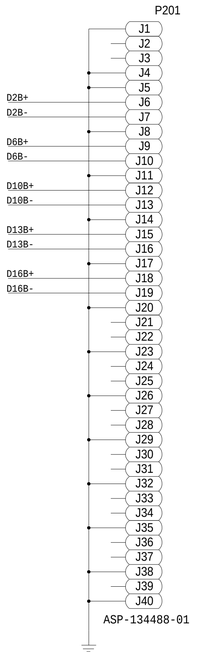


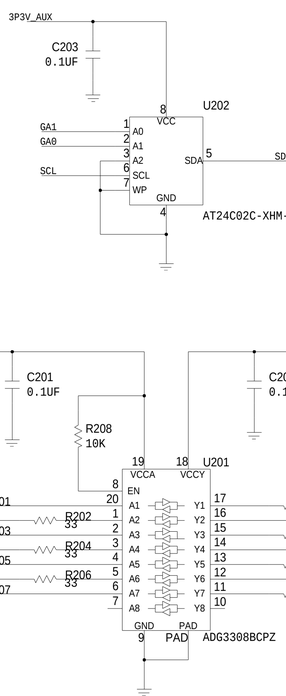


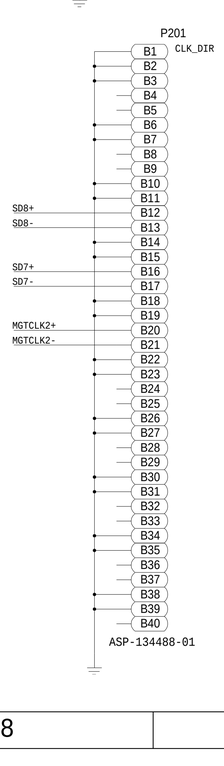


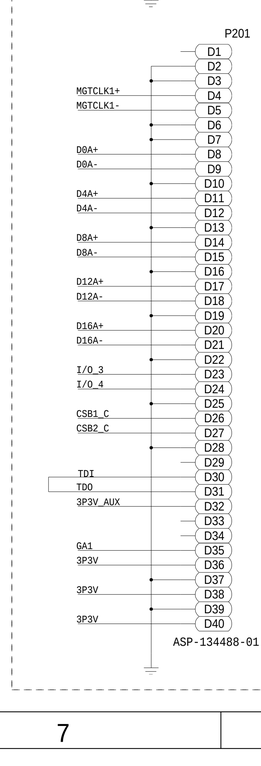
LPC

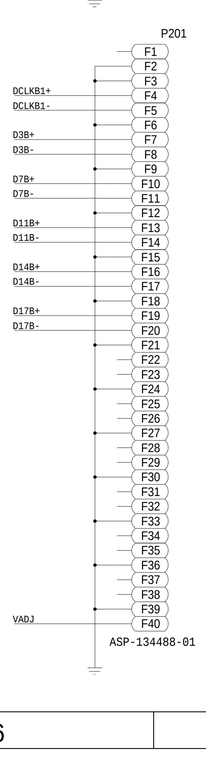


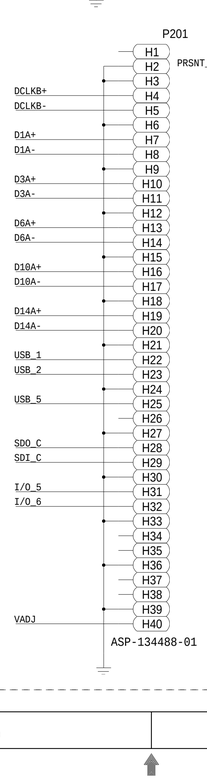


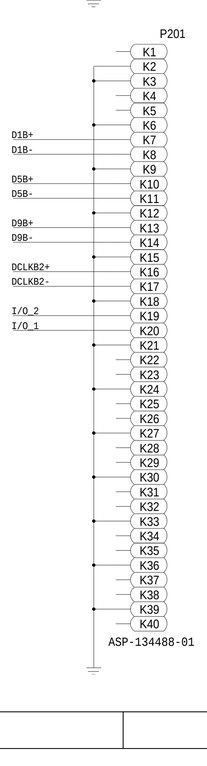












ANALOG DEVICES

SCHEMATIC

<DRAWING_TITLE_HEADER>
CVTADCFMCINTPZ
ENGINEERING BOARD

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. CVTADCFMCINTPZ01	REV B
PTD ENGINEER R. Reeder	SIZE D / SCALE NONE	SHEET 2 OF 2