ispClock™ 5400D Family

In-System Programmable, Ultra-Low Jitter Zero Delay and Fan-Out Buffer, Differential

December 2011 **Preliminary Data Sheet DS1025**

Features

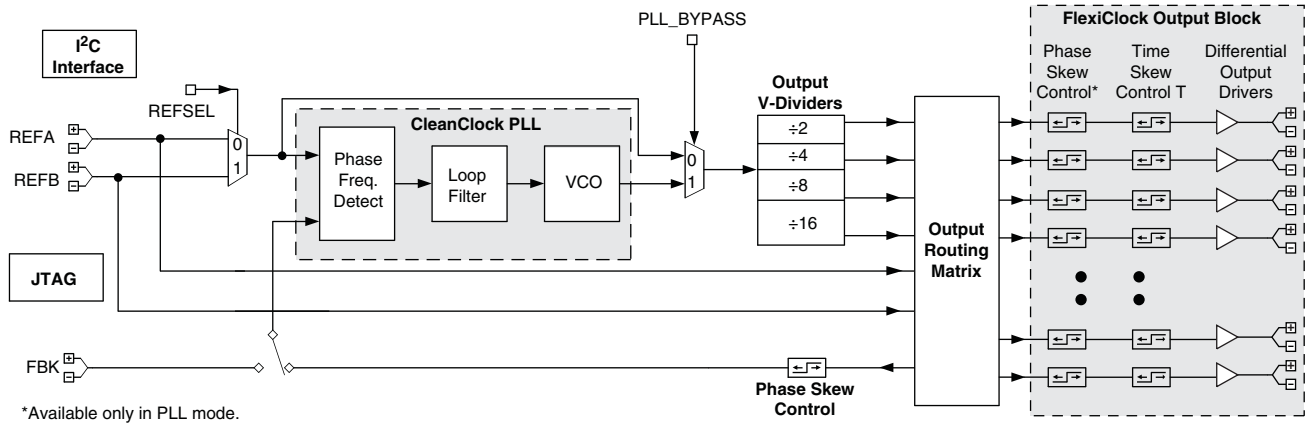
CleanClock™ PLL

- **Ultra Low Period Jitter 2.5ps**
- **Ultra Low Phase Jitter 6.5ps**
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Four output dividers
  - Programmable on-chip loop filter
  - Compatible with Spread Spectrum clocks
  - Internal/external feedback
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable differential input reference/feedback standards
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Programmable termination
  - Clock A/B selection multiplexer

FlexiClock™ I/O

- **40 MHz to 400 MHz Input/Output Operation**
- **Dual Programmable Skew Per Output**
  - Programmable phase adjustment
    - 16 settings; minimum step size 156 ps
    - Up to +/- 9.4 ns skew range
    - Coarse and fine adjustment modes
  - Programmable time delay adjustment
    - 16 settings; 18 ps
- **Dynamic Skew Control Through I^2C**
- **Low Output-to-Output Skew (<100ps)**
- **Up to 10 Programmable Fan-out Buffers**
  - Programmable differential output standards and individual enable controls
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Up to 10 banks with individual VCCO and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **All I/Os are Hot Socket Compliant**
- **Operating Modes**
  - Fan-out buffer with programmable output skew control
  - Zero delay buffer with dual programmable skew controls
- **Dynamic Reconfiguration through I^2C**
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0° to 70°C) and Industrial (-40° to 85°C) Temperature Ranges**
- **48-Pin and 64-pin QFNS Packages**
- **Applications**
  - Low-cost clock source for SERDES
  - ATCA, MicroTCA, AMC, PCI Express
  - Differential Clock Distribution
  - Generic Source Synchronous Clock Management
  - Zero-delay clock buffer

ispClock5400D Family Functional Diagram



General Description

The ispClock5400D family integrates a CleanClock PLL and a FlexiClock Output block. The CleanClock PLL provides an ultra-low-jitter clock source to a set of four V-dividers. The FlexiClock output block receives the clock output from these V-dividers through an output switch matrix and distributes them to the output pin using a programmable logic interface. There are two members in the ispClock5400D family, the ispClock5410D (10-output FlexiCLock block) and the ispClock5406D (6-output FlexiClock block). Each of the outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, SSTL, HSTL, MLVDS, HCSL) and output frequency. In addition, the skew of each of the outputs can be independently controlled. All configuration information is stored on-chip in non-volatile E^2CMOS® memory.

The ispClock5400D devices provide extremely low propagation delay (zero-delay) from input to output using the CleanClock PLL. The PLL VCO output clock frequency is divided down by a set of four V- dividers. The output frequencies from these V-dividers, $f_{VCO} \div 2$, $f_{VCO} \div 4$, $f_{VCO} \div 8$ and $f_{VCO} \div 16$ are connected to the output routing matrix. The output routing matrix enables any output pin to derive its clock from any of the V-dividers outputs. Additionally, the reference input clock can be connected directly to any output through the output routing matrix.

The FlexiClock block supports dual skew mechanisms: Phase Skew Control and Time Skew Control. These skew control mechanisms enable fixed output clock skew control during power-up and variable skew during operation.

The ispClock5400D device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The I^2C interface can be used to dynamically control the ispClock5400D configuration: Output clock frequency, Phase Skew, Time skew, Fan-out buffer mode, Output enable.

The core functions of both members of the ispClock5400D family are identical. Table 1 summarizes the ispClock5400D device family.

Table 1. ispClock5400D Family

Device	Number of Programmable Differential Clock Inputs	Number of Programmable Differential Outputs
ispClock5410D	2	10
ispClock5406D	2	6

Figure 1. ispClock5410D Functional Block Diagram

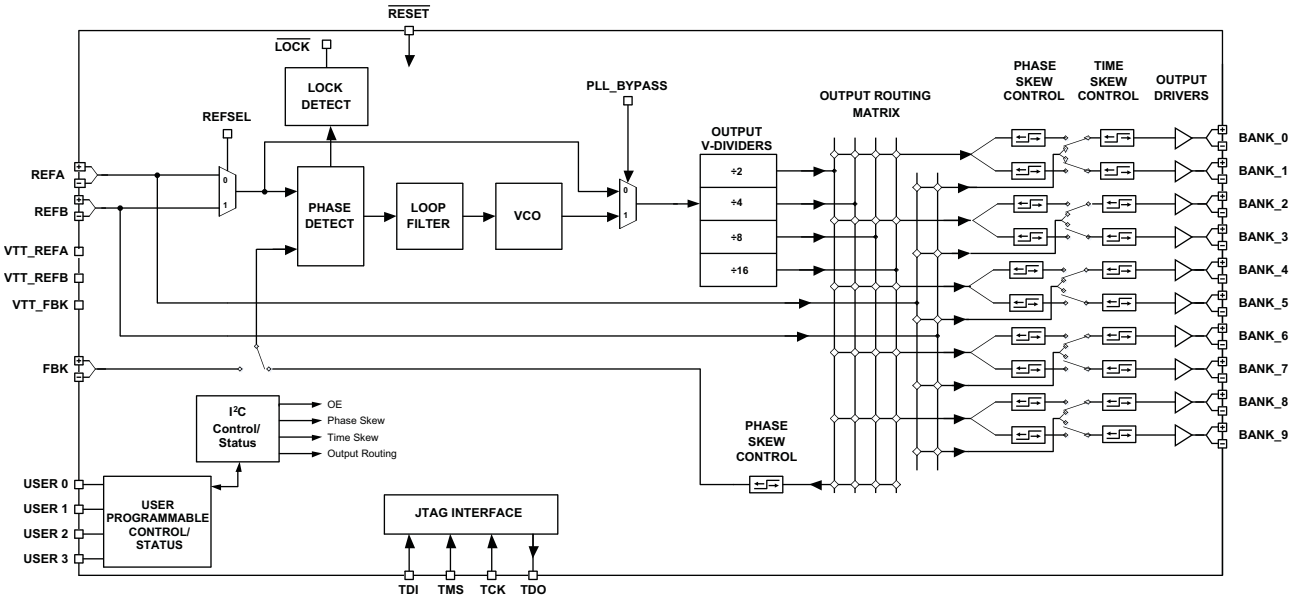
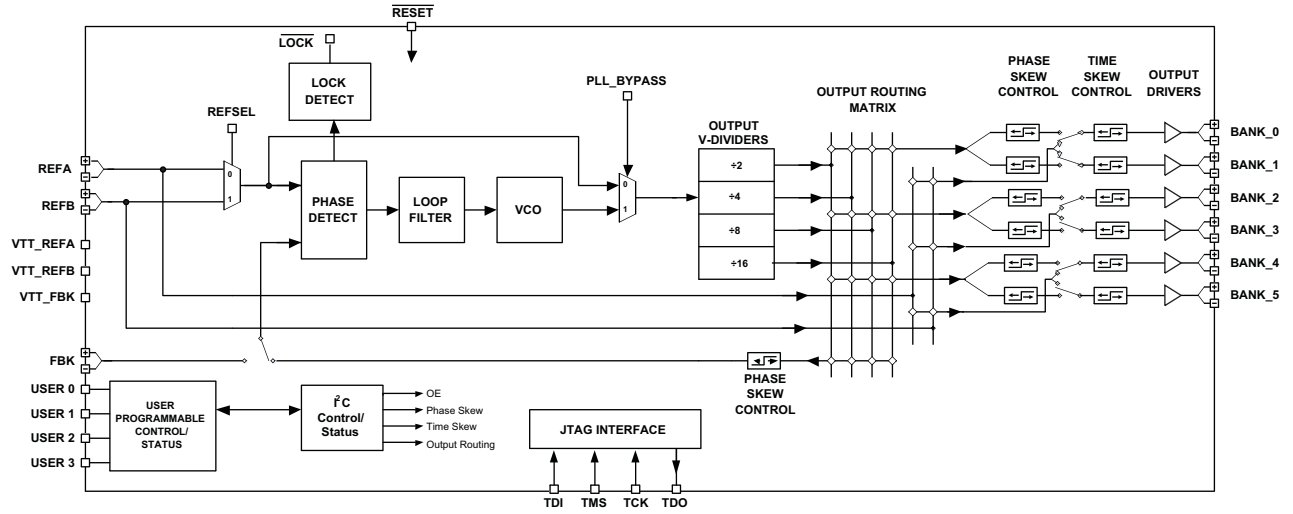


Figure 2. ispClock5406D Functional Block Diagram



Absolute Maximum Ratings

ispClock5400D

Core Supply Voltage V_{CCD} . . . . . -0.5 to 5.5V

PLL Supply Voltage V_{CCA} . . . . . -0.5 to 5.5V

JTAG Supply Voltage V_{CCJ} . . . . . -0.5 to 5.5V

Output Driver Supply Voltage V_{CCO} . . . . . -0.5 to 4.5V

Input Voltage . . . . . -0.5 to 4.5V

Output Voltage[1] . . . . . -0.5 to 4.5V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature with power supplied . . . . . -40 to 125°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		2.25	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JCOM}	Junction Temperature	Commercial	0	85	°C
T_{JIND}		Industrial	-40	100	

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
HCSL	3.135	3.3	3.465						
SSTL15	1.425	1.5	1.575	0.7	0.75	0.8		0.5 x V_{CCO}	
SSTL18	1.7	1.8	1.9	0.84	0.9	0.95		0.5 x V_{CCO}	
SSTL2 Class 1	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
HSTL Class 1	1.4	1.5	1.6	0.68	0.75	0.9		0.5 x V_{CCO}	
eHSTL Class 1	1.65	1.8	1.95	0.84	0.9	0.95		0.5 x V_{CCO}	
LVPECL	2.97	3.3	3.63						
LVDS25	2.25	2.5	2.75						
LVDS33	2.97	3.3	3.63						
MLVDS	2.25	2.5	2.75						

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	2000	V
	CDM	1000	V

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max	Units
I_{CCD}	Core Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	94	99	mA
		PLL Bypassed	65	71	mA
$I_{CCDADDER}$	Incremental ICCD Per Active Output	f_{OUT} = 400 MHz	2.8	3.2	mA
$I_{CCDADDER-TSK}$	Incremental ICCD for the First T-Skew Block		4.0	4.9	mA
$I_{CCDADDER-HCSL}$	Incremental ICCD For the First HCSL Output		4.0	5.2	mA
$I_{CCDADDER-REFB}$	Incremental ICCD Due to Active REFB INPUT	F_{IN} = 400 MHz	6.0	10	mA
I_{CCA}	Analog Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	23	30	mA
I_{CCO}	Output Driver Supply Current	Output Logic Standard = SSTL15, f_{OUT} = 400MHz	21	22	mA
		Output Logic Standard = SSTL18 f_{OUT} = 333MHz	24	27	mA
		Output Logic Standard = SSTL2 f_{OUT} = 267MHz	34	37	mA
		Output Logic Standard = HSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = eHSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = LVPECL f_{OUT} = 400MHz	20	22	mA
		Output Logic Standard = LVDS33 f_{OUT} = 400MHz	10	11	mA
		LVDS25 f_{OUT} = 400MHz	8	9	mA
		Output Logic Standard = MLVDS f_{OUT} = 266MHz	16	19	mA
		Output Logic Standard = HCSL[2] f_{OUT} = 150MHz	22	24	mA
I_{CCJ}	JTAG I/O Supply Current (Static)	V_{CCJ} = 2.5V	350	500	µA
		V_{CCJ} = 3.3V	350	500	µA

1. All unused REFCLK and FBK pins grounded. Fin = 50 MHz, internal feedback.
2. 6x HCSL current setting.

DC Electrical Characteristics – Single-Ended Logic for USER, RESET and JTAG Pins

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 1.8V[1]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	4	-4
User I/O in I²C Mode	-0.3	0.3 x V_{CCD}	0.7 x V_{CCD}	3.6V	0.4	V_{CCD} - 0.4	8	—

1. User and reset pins only.

Differential Input Characteristics (Applicable to REFA, REFB, FBK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage - LVDS		0.1	—	2.35	V
V_{THD}	Differential Input Threshold - LVDS	100mV < V_{ICM} < 300mV	±100	—	—	mV
		300mV <V_{ICM} < 2.35V	±50	—	—	mV
V_{IX}	Input Pair Differential Crosspoint Voltage	SSTL15, SSTL18, HSTL, eHSTL, LVPECL, HCSL	0.3		2.35	V

Output Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	R_T = 100Ω	—	1.375	1.6	V
V_{OL}	Output Low Voltage	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100Ω	250	400	450	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.1	1.2	1.375	V
ΔV_{OS}	Change in V_{OD} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND, LVDS25	—	—	24	mA
		V_{OD} = 0V, Outputs Shorted to GND, LVDS33			35	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	5	mA
DC_{CKOUT}	Output Clock Duty Cycle		48		52	%
DC-ERROR	Error in Duty Cycle[1]	LVDS25 (Figure 3)	-50		50	ps
		LVDS33 (Figure 3)	-65		65	ps
t_{RF}	Rise and Fall Time[1]	LVDS25 (Figure 3)	250		550	ps
		LVDS33 (Figure 3)	260		400	ps

1. Measured at f_{OUT} = 400 MHz.

Output Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.1	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.20	—	2.42	V
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.86	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.44	—	1.68	V
V_{OD}	Output Voltage Differential		0.6	—	1	V
DC_{CKOUT}	Output Clock Duty Cycle[2]	Figure 3	47		53	%
t_{RF}	Rise and Fall Time[2]	Figure 3	300		400	ps

1. 100Ω differential termination.
2. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL15

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OH} = -8mA	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OL} = 8mA			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	350		460	ps

1. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -9mA, V_{CCO} = 1.7V	1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 9mA, V_{CCO} =1.7V			0.6	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	$V_{CCO}/2$ - 0.05		$V_{CCO}/2$ + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	230		380	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{CCO} = 2.3V	1.74			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CCO} = 2.3V			0.56	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	V_{REF} - 200 mV		V_{REF} + 200 mV	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	260		400	ps

1. Measured at f_{OUT} = 267 MHz.

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.4V	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.4V			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 5	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 5	300		460	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.65V	V_{CCO} - 0.45			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.65V			0.45	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 5	V_{CCO}/2 - 0.05		V_{CCO}/2 + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 5	250		400	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – MLVDS

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage Magnitude	Figure 8b	480		650	mV
ΔV_{OD}	Change in Differential Output Voltage Magnitude Between Logic States	Figure 8b	-50		+50	mV
V_{OS}	Output Voltage Offset	Figure 8a	1		1.4	V
ΔV_{OS}	Change in V_{OS} Between H and L		-50		50	mV
V_{OC}	Output Open Circuit Steady State Voltage		0		2.4	V
I_{SAB}	Output Short Circuit Current, Outputs Shorted				24	mA
I_{SA}	Output Short Circuit Current	Figure 8c			43	mA
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 4	48		52	%
t_{RF}	Rise and Fall Time[1]	Figure 4	280		510	ps

1. Measured at f_{OUT} = 266 MHz.

Electrical Characteristics – HCSL

Symbol	Description	Conditions	Min.	Max.	Units
V_{OX}	Output Differential Pair Crosspoint Voltage	Crossing Point at Max. Swing of 0.7V	250	550	mV
ΔV_{OX}	V_{OX} Variation Across All Edges			140	mV
V_{OH}	Output High Voltage	Figure 7	1.3		V
t_R	Edge Rate Rising	Differential[1] (Figure 7)	0.6	4	V/ns
t_F	Edge Rate Falling	Differential[1] (Figure 7)	0.6	4	V/ns

1. Differential output signal, ±150mV from 0V crossing.

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	USER[3:0], Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	USER[3:0]	—	80	120	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	5	7	pF
		Note 1	—		8	pF

1. Applies to clock reference inputs and feedback inputs when termination ‘open’.
2. Applies to TDI, TDO, TMS and $\overline{\text{RESET}}$ inputs.
3. Applies to USER[0..3] pins.
4. Applies to all logic types when in tristated mode.
5. Applies to TCK, $\overline{\text{RESET}}$ and USER inputs.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOO} Output Adders[1, 2]					
SSTL2_out	Output Configured as SSTL2 Buffer		0.4		ns
SSTL18_out	Output Configured as SSTL18 Buffer		-0.6		ns
SSTL15_out	Output Configured as SSTL15 Buffer		-0.5		ns
HSTL_out	Output Configured as HSTL Buffer		-0.5		ns
eHSTL_out	Output Configured as eHSTL Buffer		-0.6		ns
MLVDS_out	Output Configured as MLVDS Buffer		0.25		ns
HCSL_out	Output Configured as HCSL		0.35		ns
LVDS25_out	Output Configured as LVDS25		0.25		ns
LVPECL_out	Output Configured as LVPECL		0		ns

1. Measured under standard output load conditions, see Figures 3 to 8.
2. All output adders referenced to LVDS33.

Output Test Loads

Figures 3 to 8 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3. LVDS/LVPECL Termination Load

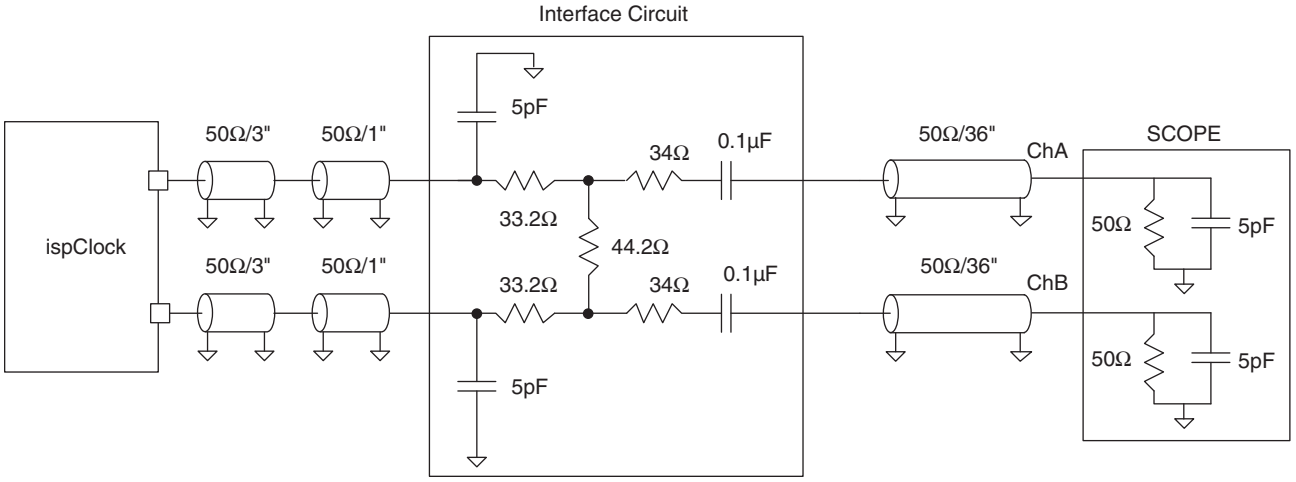


Figure 4. MLVDS Termination Load

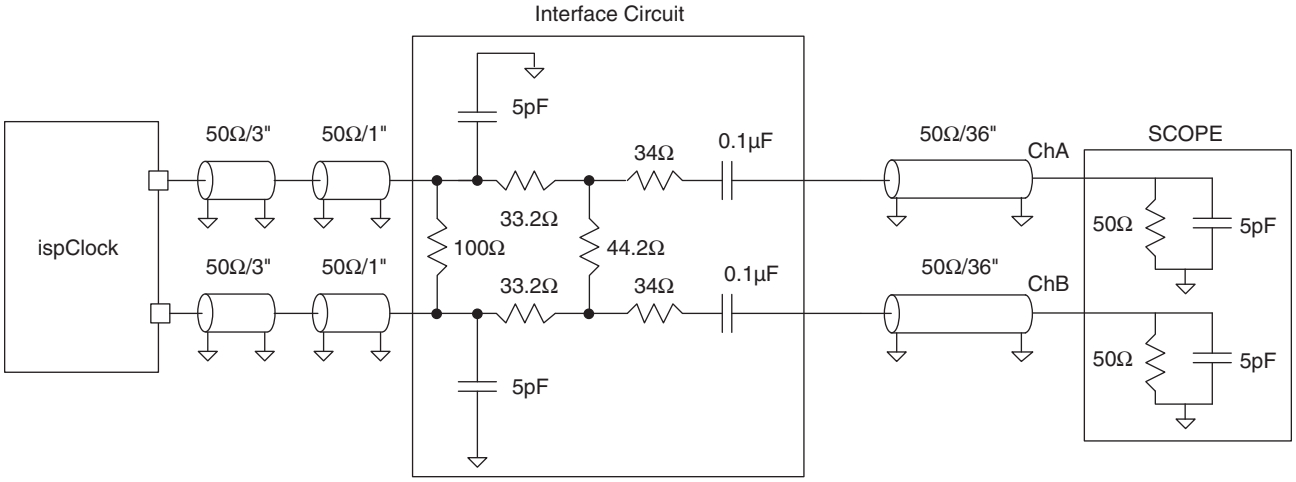


Figure 5. Differential HSTL Termination Load

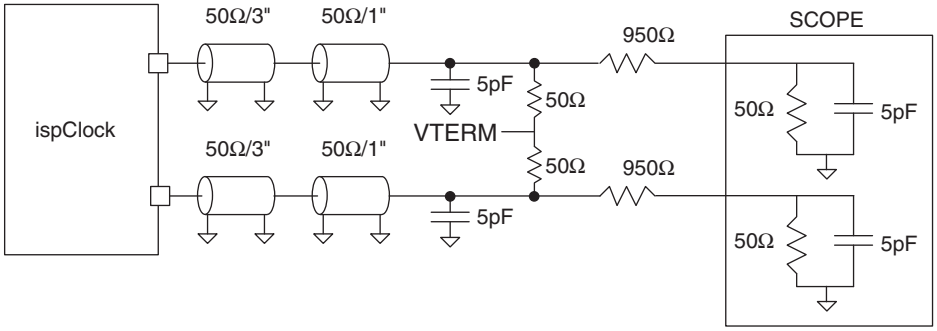


Figure 6. Differential SSTL Termination Load

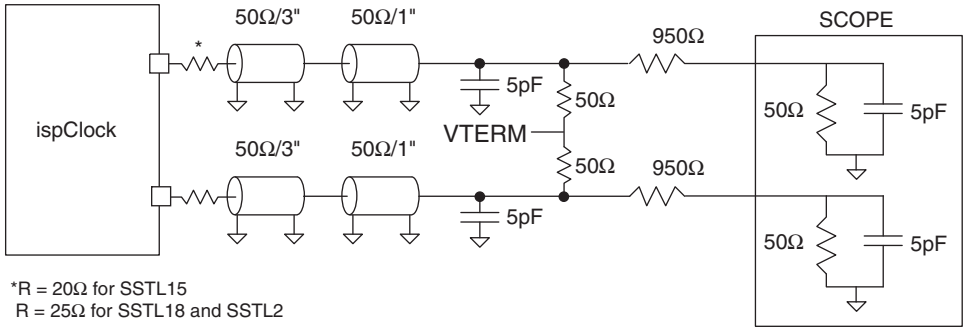


Figure 7. HCSL Termination Load

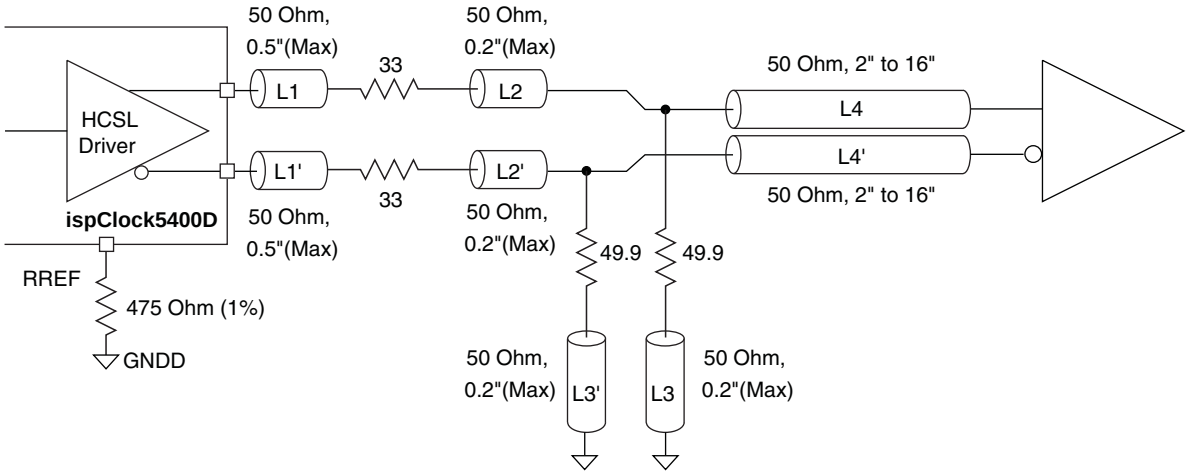
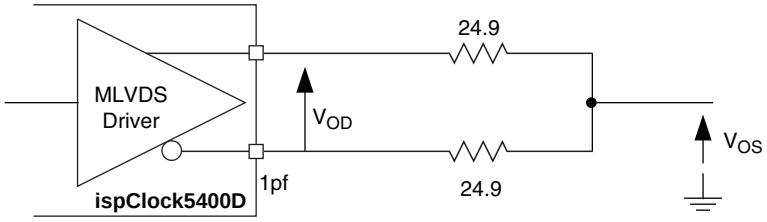
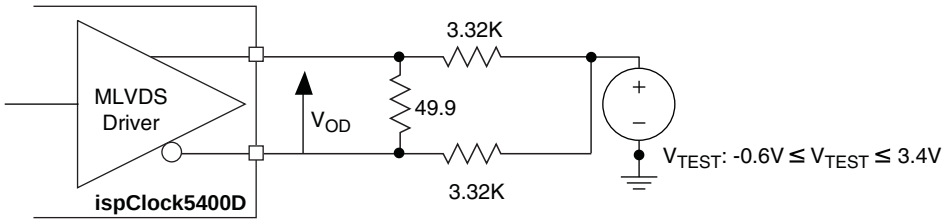


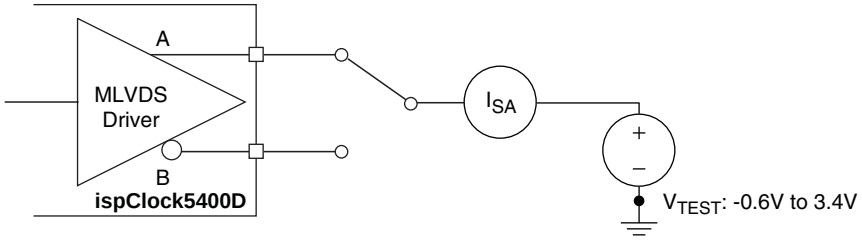
Figure 8. MLVDS Termination Load



(a) Common Mode Output Voltage Test Circuit



(b) Differential Output Voltage Test Circuit



(c) Short Circuit Curreent (I_{SA}) Test Circuit

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and Feedback Input Frequency Range		40[1]		400[7]	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and Feedback Input Clock HIGH and LOW Times		900			ps
t_{RINP}, t_{FINP}	Reference and Feedback Input Rise and Fall Times	Measured Between 20% and 80% Levels			5	ns
f_{PFD}	Phase Detector Input Frequency Range		40		400[7]	MHz
f_{VCO}	V_{CO} Operating Frequency		400		800	MHz
V_{DIV}	Output Divider Range (Power of 2)		2		32	
f_{OUT}	Output Frequency Range[1]	Fine Skew Mode	25		400[5]	MHz
		Coarse Skew Mode	12.5		200[5]	MHz
t_{JIT} (cc)	Output Adjacent-Cycle Jitter[4] (1000-Cycle Sample)				29	ps (p-p)
t_{JIT} (per)	Output Period Jitter[4] (10000-Cycle Sample)				2.5	ps (RMS)
$t_{JIT(\phi)}$	Reference Clock to Feedback Jitter (2000-Cycle Sample)[6]			6.5		ps (RMS)
$t\phi$	Static Phase Offset[3]	PFD Input Frequency ≥ 100MHz	-5	45	95	ps
$t\phi_{DYN}$	Dynamic Phase Offset	Spread Spectrum Modulation Index = -0.5%			50	ps
t_{PD_FOB}	Reference to Output Propagation Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Disabled		6		ns
$t_{PD\_FOB\_TS\_EN}$	Reference to Output Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Enabled		7		ns
t_{DELAY}	Reference to Output Delay with Internal Feedback Mode[2]	V=2		4		ns
t_{LOCK}	PLL Lock Time	From Power-up Event		2.5	15	ms
t_{RELOCK}	PLL Relock Time	$f_{IN} = f_{OUT}$ = 100 MHz		2.5		ms

1. In PLL Bypass mode (PLL_BYPASS = HIGH), input and output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Input and outputs LVPECL mode
3. Inserted feedback loop delay < 5ns
4. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVDS, internal feedback.
5. Also dependent on output type.
6. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVPECL, external feedback.
7. In Coarse Skew Mode, maximum input frequency is 200MHz.

Timing Specifications

Skew Matching[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-Output Skew	Between any two identically configured and loaded outputs, regardless of bank, on the same device.	—	—	75	ps
$t_{SKEW-FOB}$		T-skew Disabled			75	ps
$t_{SKEW-FOB-TS-EN}$		T-skew Enabled			100	ps

1. LVPECL outputs.

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{PSKRANGE}$	Phase Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 400 MHz	—	4.68	—	ns
		Fine Skew Mode, f_{VCO} = 800 MHz	—	2.34	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	9.38	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	4.68	—	
PSK_{STEPS}	Phase Skew Steps per Range		—	16	—	
$t_{PSKSTEP}$	Phase Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 400 MHz	—	312	—	ps
		Fine Skew Mode, f_{VCO} = 800 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	625	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	312	—	
t_{PSKERR}	Phase Skew Time Error at Any Skew Setting[3]	Fine skew mode	—	10	—	ps
		Coarse skew mode	—	10	—	

1. Skew control range is a function of V_{CO} frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of V_{CO} frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Programmable Skew Control – Time Skew

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
$t_{T-SK-RANGE}$	Time-Skew Control Range		—	270	—	ps
$t_{SK-STEPS}$	Number of Time-Skew Steps		—	16	—	ps
$t_{T-SK-STEP}$	Time-skew Step Size		—	18	—	ps
$t_{T-SKERR}$	Step Size Error at Any Skew Setting		—	5	—	ps

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, OEb or GOEb to Output Disabled/Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{\text{RESET}}$ Pulse Width		10	—		µs
RST_SLEW	Reset Signal Slew Rate				1	V/µs

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I²C clock/data rate		100		400	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

Timing Diagrams

Figure 9. Erase (User Erase or Erase All) Timing Diagram

Figure 10. Programming Timing Diagram

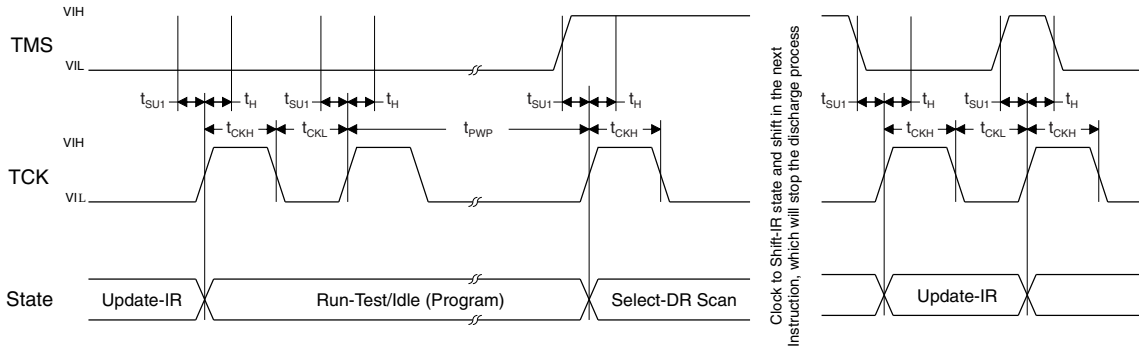


Figure 11. Verify Timing Diagram

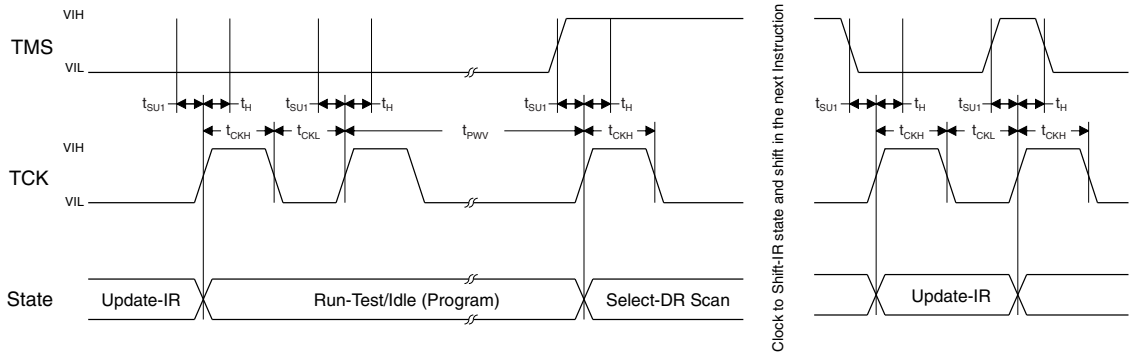
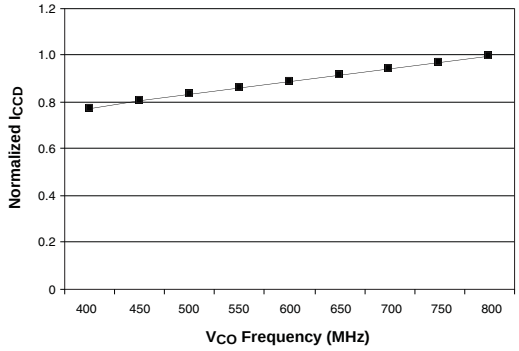


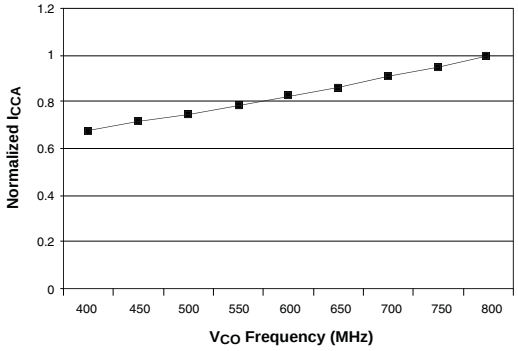
Figure 12. Discharge Timing Diagram

Typical Performance Characteristics

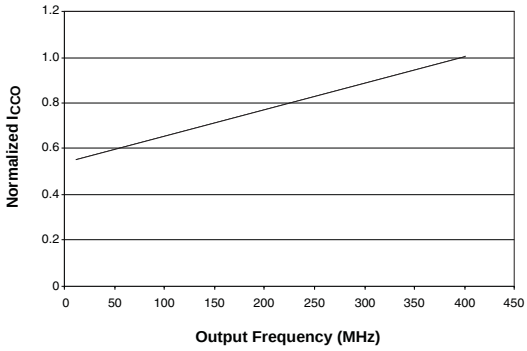
Normalized I_{CCD} vs. V_{CO} Frequency (I_{CCD} Value Normalized to V_{CO} at 800 MHz)



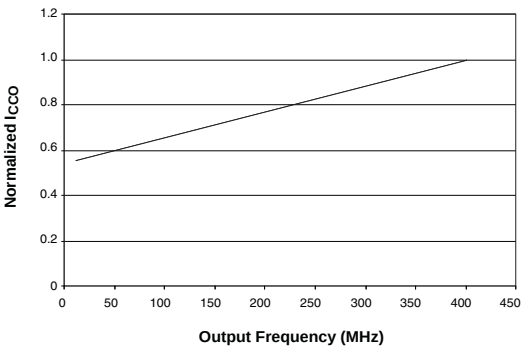
Normalized I_{CCA} vs. V_{CO} Frequency (I_{CCA} Value Normalized to V_{CO} at 800 MHz)



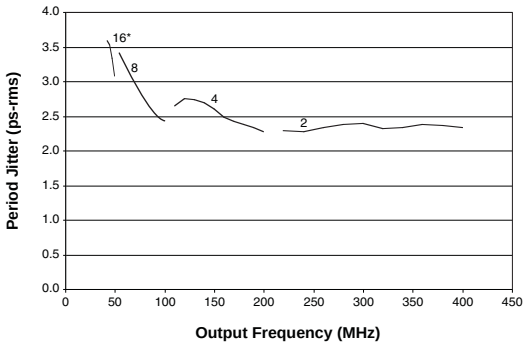
Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVDS33)



Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVPECL)

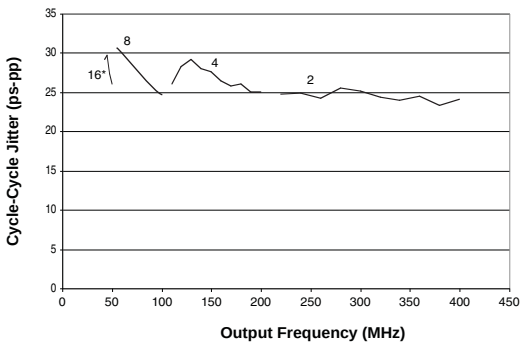


Period Jitter vs. Output Frequency



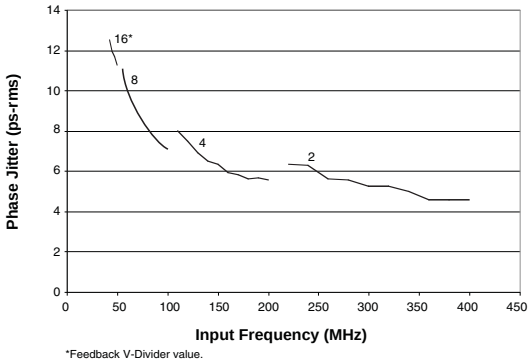
*Feedback V-Divider value.

Cyle-Cycle Jitter vs. Output Frequency



*Feedback V-Divider value.

Phase Jitter vs. Input Frequency



*Feedback V-Divider value.

Detailed Description

CleanClock PLL

The ispClock5400D provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the CleanClock PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Any of the frequencies from the 4-output V-divider can be used as feedback to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5400D provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter. The output of the loop filter controls the VCO.

A lock-detection feature is also associated with the PFD. When the ispClock5400D is in a LOCKED state, the LOCK output signal is asserted (programmable high or low). The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256. The LOCK output from the PFD can be routed to one of the USER Programmable pins.

When the lock condition is lost the LOCK signal will be de-asserted immediately.

Loop Filter: The loop filter parameters are automatically selected by the PAC-Designer software depending on the feedback V-divider setting.

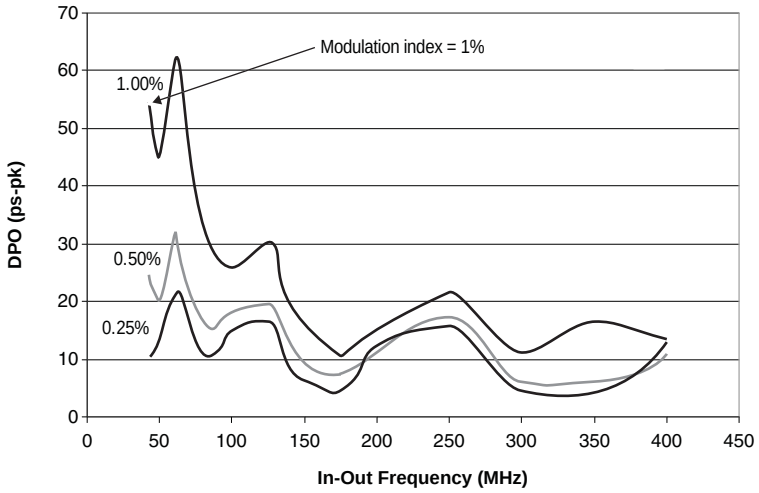
Spread Spectrum Support: The reference clock inputs of the ispClock5400D device are spread spectrum clock compatible. The tolerance limits are:

- Center spread ±0.125% to ±0.25%
- Down spread -0.25% to -0.5%
- 30-33kHz modulation frequency

Table 2. PLL Bandwidth

V-Divider	Bandwidth (MHz)
2	9.8
4	7.0
8	4.5
16	2.4

Figure 13. Dynamic Phase Offset (DPO)



VCO

The operating frequency of the on-chip VCO of the ispClock5400D ranges from 400MHz to 800MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to set the phase skew step size. Using the VCO as the basis for controlling output phase skew allows for highly precise and consistent phase skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V-dividers

The ispClock5400D incorporates a set of four dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input. The division values of these V-dividers are set to 2, 4, 8 and 16. In Coarse Skew Mode, the division values are set to 4, 8, 16 and 32.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V-divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_K is the frequency of V-divider k
f_{REF} is the input reference frequency
V_{FBK} is the division ratio of the V-divider used to close the PLL feedback path
V_K is the output divider K

Note that because the feedback may be taken from any V-divider, V_k and V_{fbk} may refer to the same divider.

PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V-dividers. The output frequency for a given V-divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and phase skew generation are unavailable. The PLL can be bypassed through I^2C or through the USER pins.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output bank. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable phase skew feature for the feedback path is available in the internal feedback mode. However, both phase and time skew features are available for the feedback path in the external feedback mode.

Reference and External Feedback Inputs

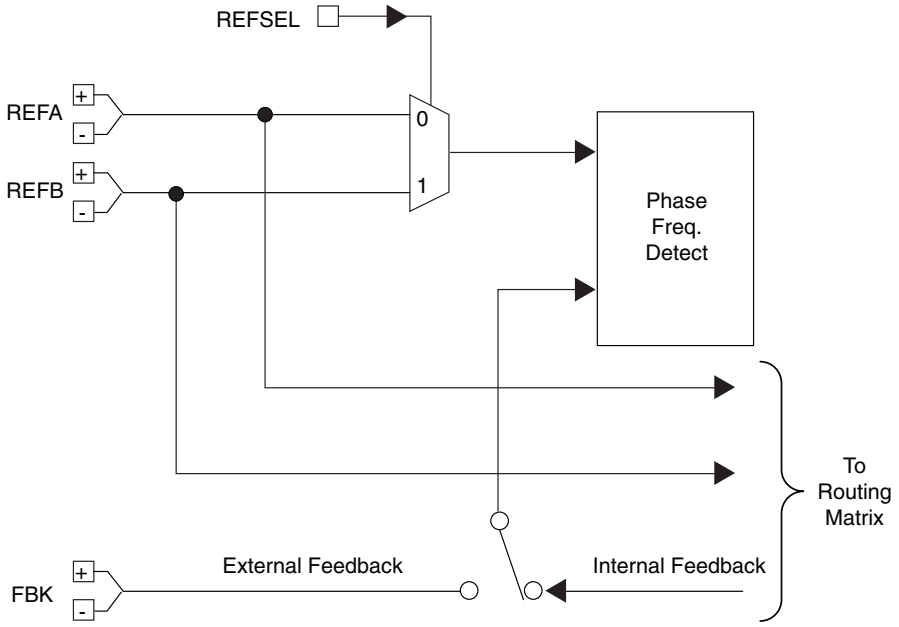
The ispClock5400D provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins (REFA, REFB) can be interfaced with two differential clocks. The active clock selection control through REFSEL signal. The REFSEL signal can be driven either by one of the USER pins or through the I^2C interface.

Supported input logic reference standards:

- LVDS
- LVPECL
- SSTL2
- SSTL18
- SSTL15
- HSTL
- eHSTL
- HCSL
- LVCMOS

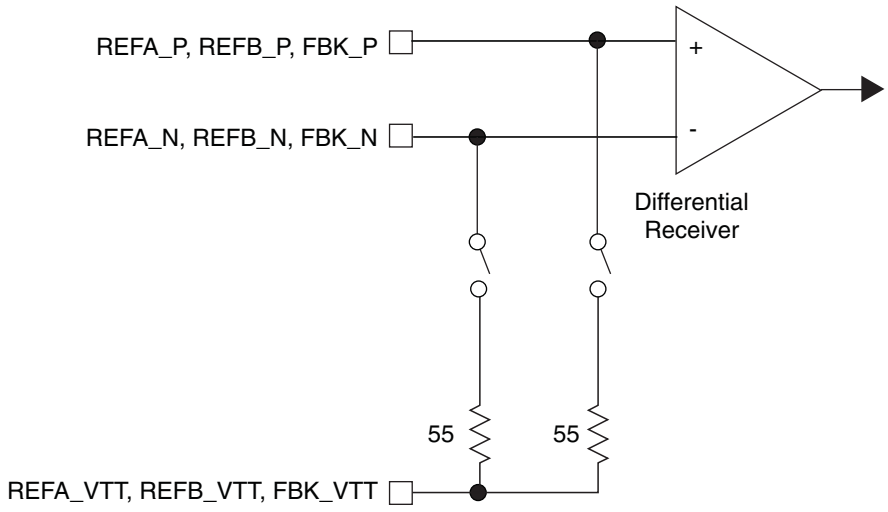
Figure 14. Reference and Feedback Input



Input Receiver Termination Configuration

Each input features internal 55 Ohm termination resistors as shown in Figure 15. The REFA, REFB and FBK inputs terminate to REFA_VTT, REFB_VTT, and FBK_VTT respectively. If external termination resistors are used, these internal termination resistors can be disconnected through PAC-Designer software.

Figure 15. Input Receiver Termination Configuration

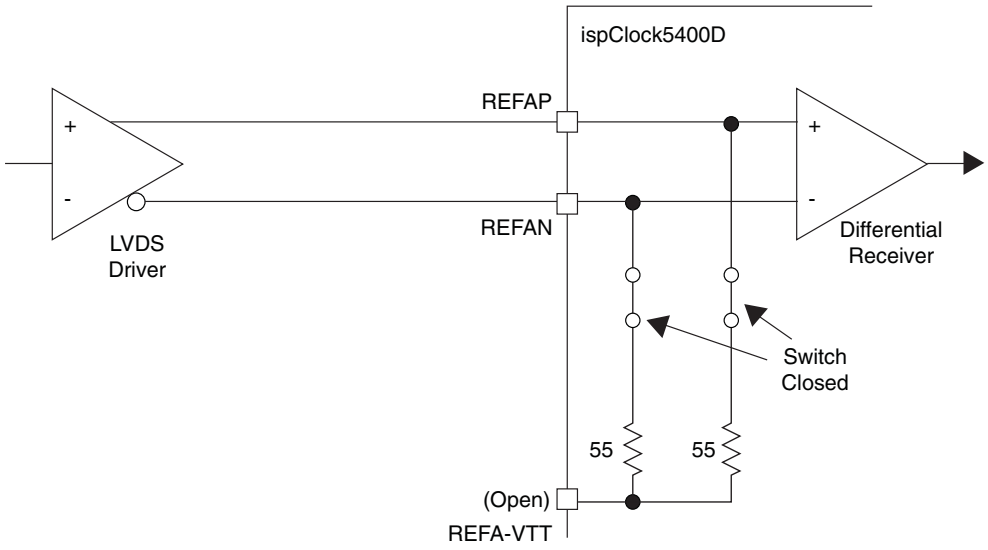


The following usage guidelines are suggested for interfacing to supported logic families.

LVPECL/LVDS

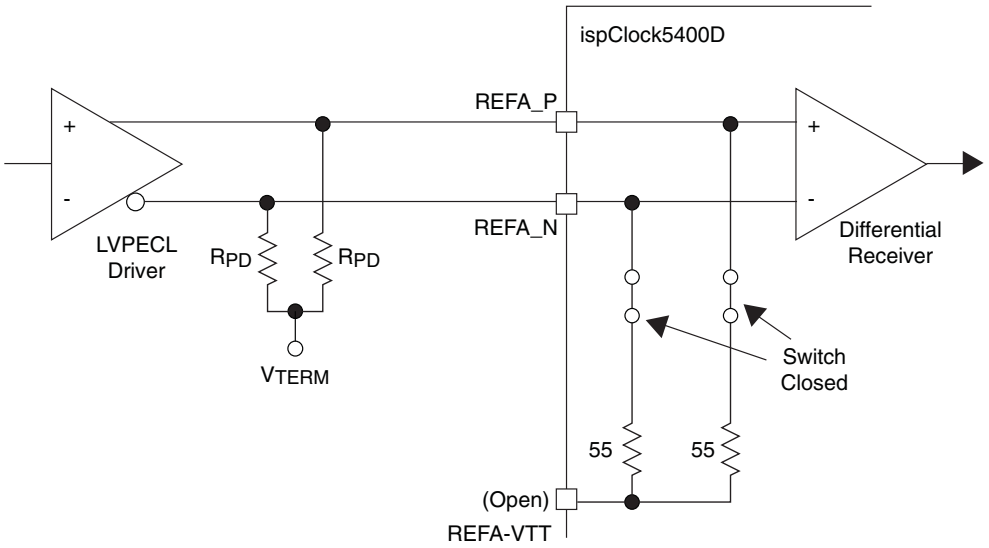
Both termination resistors in the receiver should be engaged. The VTT pin should be left floating. This creates a floating 110Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 16.

Figure 16. LVDS Input Receiver Configuration



Note that while a floating 110Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 17)

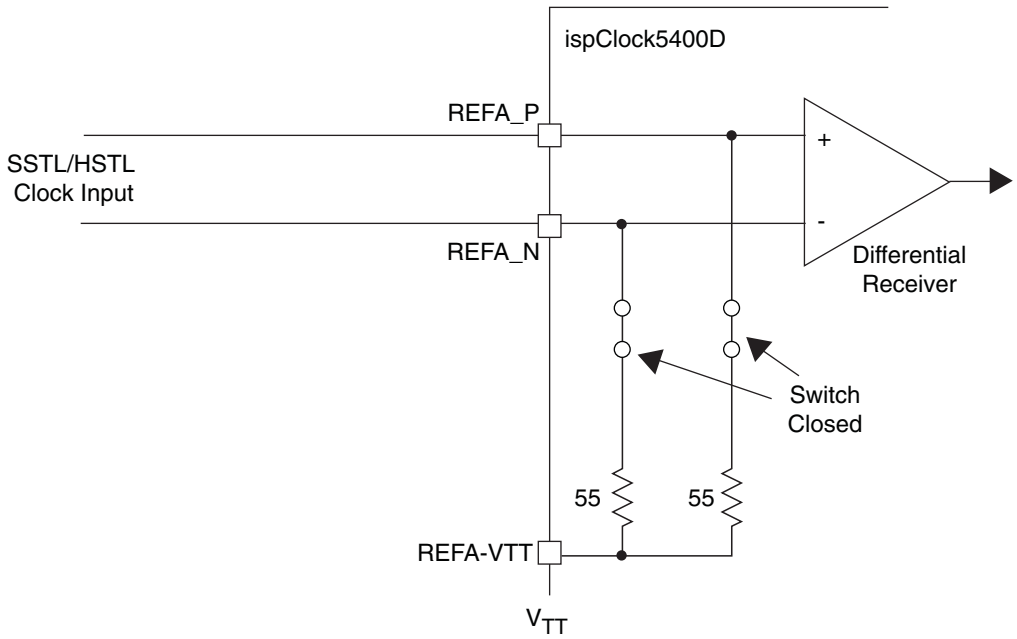
Figure 17. LVPECL Input Receiver Configuration



SSTL/HSTL

To interface the ispClock5400D with the SSTL or HSTL signals, close the switch connecting the REFP and REFN signals to termination resistors. Connect the VTT pin to a voltage half of the supply voltage of the clock input.

Figure 18. SSTL/HSTL Input Receiver Configuration

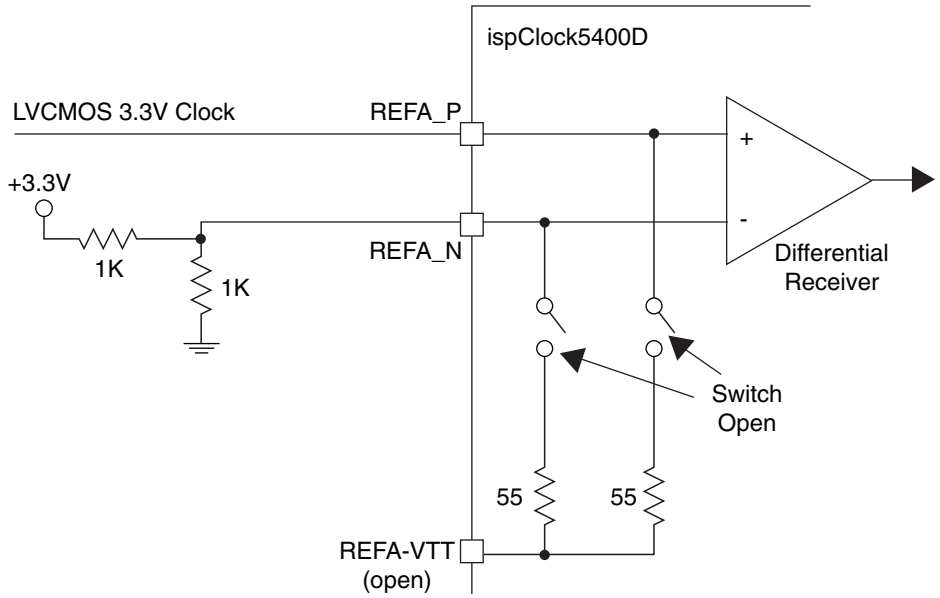


LVCMOS

The ispClock5400D input section can be connected to single ended signals such as the LVCMOS3.3V by connecting it directly to REFAP pin while the threshold is provided by the REFAN terminal at 1.65V (= 3.3V ÷ 2). The threshold reference voltage can be derived by a potential divider using 2, 1K ohm resistors.

Note: To minimize the noise injection into the receiver, the 3.3V at the input of the potential divider should be sufficiently filtered. The GND limb of the potential divider should be connected to the GND pin of the source.

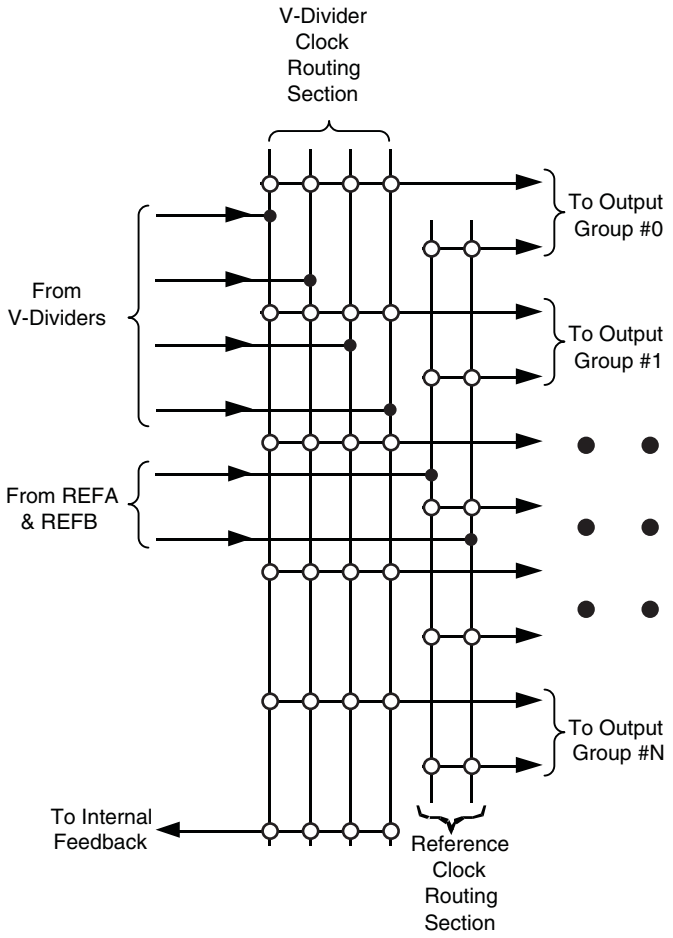
Figure 19. LVCMOS Input Receiver Configuration



Output Routing Matrix

There are two sections in the Output Routing Matrix: the V-divider clock routing section and the REF clock routing section. The V-divider routing section enables connecting any output group and the internal feedback path to any of the output V-dividers. The Ref clock routing section can route either of the Ref clocks to any output group.

Figure 20. ispClock5400D Output Routing Matrix



FlexiClock Output Section

The FlexiClock output block distributes clock received from the Output Routing Matrix. The signalling interface of each of the differential clock outputs can be individually programmed. The output voltage swing is controlled by the associated output VCC and GND pins. The VCCO, the GNDO and the associated differential clock output pair is called an output bank.There are six output banks in the FlexiClock output section in the ispClock5406D device. The FlexiClock output section the ispClock5610D supports 10 output banks.

Output Groups

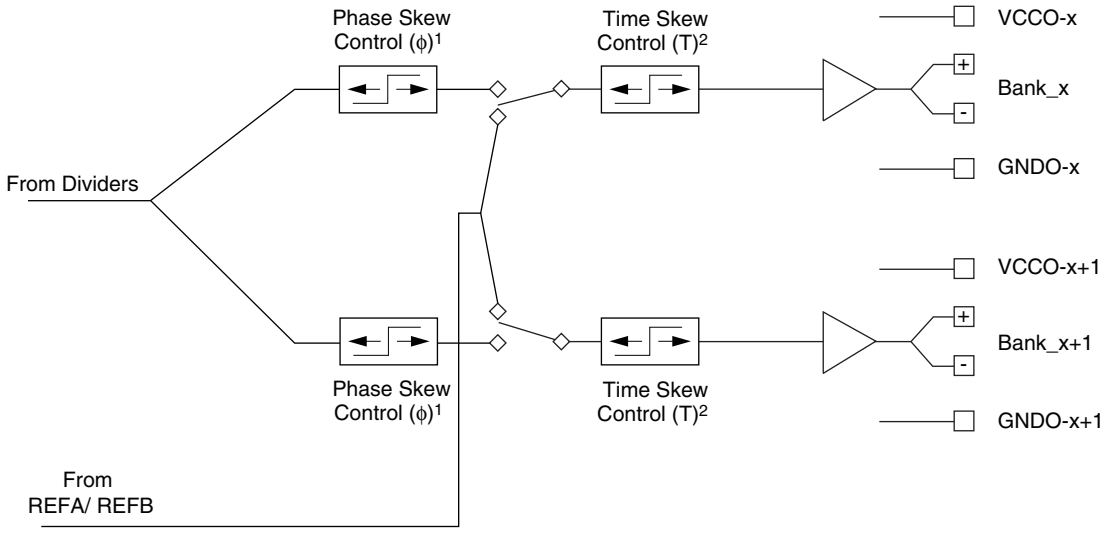
The ispClock5400D provides multiple banks, with each bank supporting a high-speed clock output and the associated VCCO and GND pins. Two adjacent banks form an Output Group (Bank 0 and Bank 1 belong to Group #0, Bank 2 and Bank 3 belong to Group #2, and so on). There are ten banks (five Output Groups) in the ispClock5410D and three output groups in the ispClock5406D device. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by USER pins or through I^2C. Additionally, each bank output clock can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 21 shows a block diagram of an ispClock5400D Output Group and its associated skew control. The two outputs in an Output Group share the connection to the Output Routing Matrix.

Because of the high edge rates which can be generated by the ispClock5400D clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respec-

tive output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDO pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 21. ispClock5400D Output Group and Skew Control



1. Phase Skew Control mechanism is applicable only to outputs connected to one of the V-dividers and when PLL is active.
2. Time Skew Control mechanism is applicable to all outputs.

Each clock output from the output group (Figure 21) can be connected to either reference clock or to a V-divider clock. However, both outputs can source only from the same V-divider output or the same reference clock at any time.

The ispClock5400D supports two skew controls: Phase Skew Control (ϕ) and Time Skew Control (T).

The Phase Skew Control mechanism is available only on outputs connected to the V-divider clocks because the Phase Skew Control timing is derived from the VCO. The Phase skew of each output of an Output Group can be individually adjusted.

The Time Skew Control mechanism derives the skew control timing from internal delay lines. The time skew mechanism is available on outputs connected to the V-dividers as well as outputs connected to reference clocks.

The output skew of the clocks connected to the V-dividers can be adjusted by both phase skew and time skew controls.

Each of the ispClock5400D's output driver banks can be configured to support the following logic outputs:

- LVDS
- LVPECL
- SSTL15
- SSTL18
- SSTL2
- HSTL
- eHSTL
- MLVDS
- HCSL

Skew Control Units

The ispClock5400D supports two skew control mechanisms: Phase Skew Control and the Time Skew Control. The Phase Skew Control mechanism delays the output clock by altering its phase angle. The Time Skew control mechanism delays the output clock by delay lines. There are 16 steps of Time Skew and Phase Skew available for each output clock.

Phase Skew Control Units

Each of the ispClock5400D's clock outputs is supported by the Phase Skew Control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

The ispClock5400D's phase skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. Because the skew time step is determined by the VCO period, the resultant output skew increment/ decrement is equivalent to changing the phase angle of the output clock. The phase skew is measured in terms of 'Phase Unit Delay' (PUD) and represented in nanoseconds. Each output can be individually delayed by up to 15 PUD. The ispClock5400D family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 156 to 312ps, while in the coarse skew mode unit skew varies from 312 to 625ps. The exact value phase unit delay may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

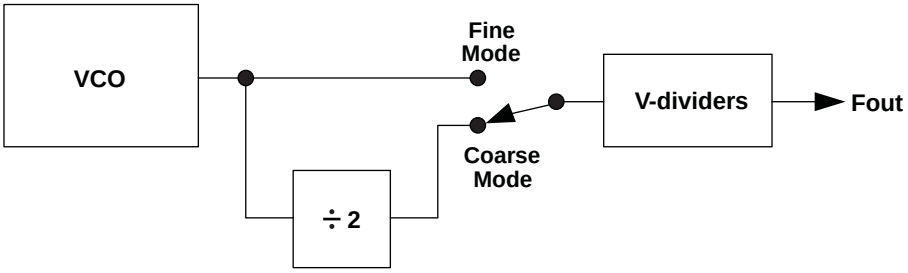
For fine skew mode, $PUD = \frac{1}{8f_{vco}}$ For coarse skew mode, $PUD = \frac{1}{4f_{vco}}$ (5)

Please note that Phase Skew Control is only usable when the PLL is not in bypass mode. In PLL bypass mode, output phase skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay, the time skew delay setting, and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5400D family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides phase unit delay ranging from 312ps (f_{VCO} = 800MHz) to 625ps (f_{VCO} = 400MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 22. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (400MHz to 800MHz).

Figure 22. Additional Factor-of-2 Division in Coarse Mode



When one moves from fine skew mode to coarse skew mode with a given divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (400MHz to 800MHz). This can be accomplished by changing the feedback to the next lower V-divider. All output frequencies will remain unchanged from what they were in fine mode.

Note: Avoid exceeding maximum f_{VCO} when changing skew control between fine and coarse modes.

Time Skew Control Unit

The Time Skew Control mechanism can insert an individually programmable delay into every clock output signal in addition to Phase Skew Control Delay. The Time Skew Control is applicable to outputs configured as Non-Zero Delay Buffers. For outputs configured as Zero Delay Buffer, the Time Skew Control can be used to fine tune the de-skew delay to compensate for the differences in clock trace lengths.

The ispClock5400D provides programmable steps of Time Skew for each output through a 16-step programmable delay line per output. The step size of this delay line, called 'Time Unit Delay' (TUD) is specified by the $t_{T\text{-}SK\text{-}STEP}$ parameter.

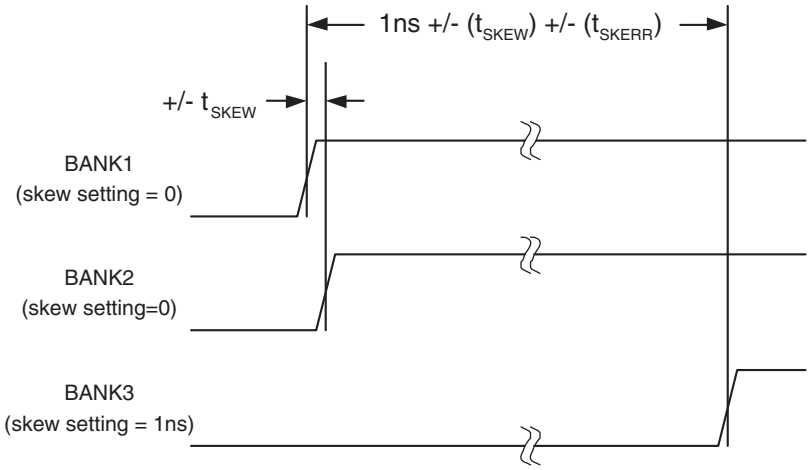
Note: Time Skew step size does not change with the VCO operating frequency.

Output Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5400D family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by the t_{SKEW} parameter. In Figure 23 the Bank1 and BANK2 outputs show the skew error between two matched outputs.

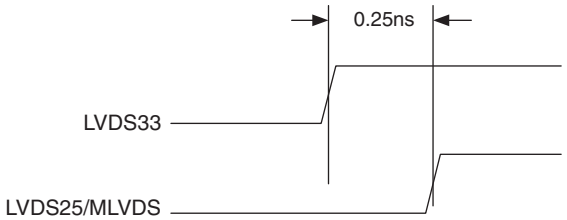
Figure 23. Skew Matching Error Sources



One can also program a user-defined skew between two outputs using the phase or Time Skew Control units. The typical error for any non-zero skew setting is given by the t_{PSKERR} and $t_{T\text{-}SKERR}$ specification. For example, if one is in fine skew mode with a VCO frequency of 500MHz, and selects a skew of 4PUD, the realized skew will be 1ns, which will typically be accurate to within +/-10ps. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1 and Bank3 outputs in Figure 23 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t_{IOO} output adders specified in the table 'Switching Characteristics'. That table specifies the additional skew added to an output using LVDS33 as a baseline. For instance, if one output is specified as LVDS25, it has a delay adder relative to LVDS33 of 0.25ns. If another output is specified as MLVDS, then one would expect 0ns of additional skew between the two outputs due to this adder. This timing relationship is shown in Figure 24.

Figure 24. Output Timing Adders for Logic Type

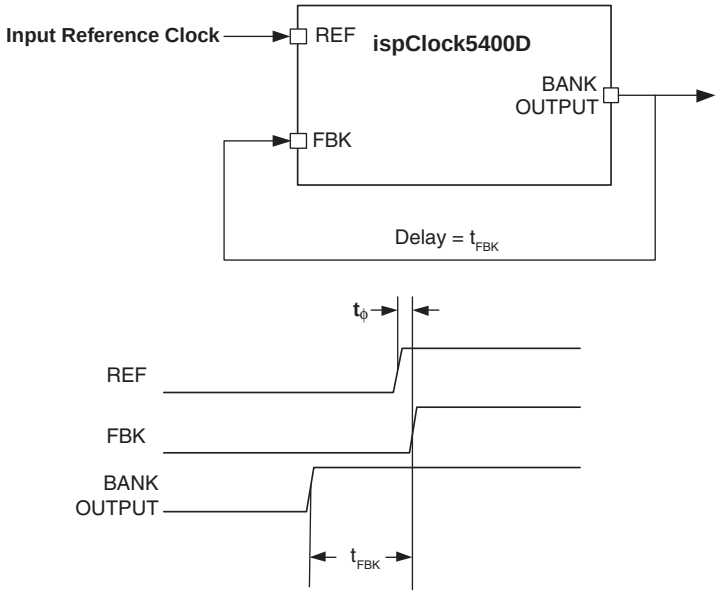


By selecting the same feedback logic type and clock output, the output delay adders for the clock output are automatically compensated for.

Static Phase Offset and Input-Output Skew

The ispClock5400D's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. Using external feedback (Figure 25), the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase offset. Note that any propagation delay (t_{FBK}) in the external feedback path drives the phase of the output signal *backwards* in time with respect to input clock phase. For this reason, if zero input-to-output delays are required, the length of the signal path between the output pin and the feedback pin should be minimized.

Figure 25. External Feedback Mode and Timing Relationships



ispClock5400D Configurations

The ispClock5400D device can be configured to operate in several modes, including:

- Zero Delay Buffer Mode
- Mixed Zero Delay and Non-Zero Delay Buffer Mode
- Dual Non-Zero Delay Buffer Mode
- Non-Zero Delay Buffer Mode With and Without Output Dividers

The output routing matrix of the ispClock5400D provides up to six independent any-to-any paths from inputs to output pairs:

- From any V-dividers to any Output Group in ZDB mode or PLL Bypass modes
- From either REFA or REFB inputs to any Output Group

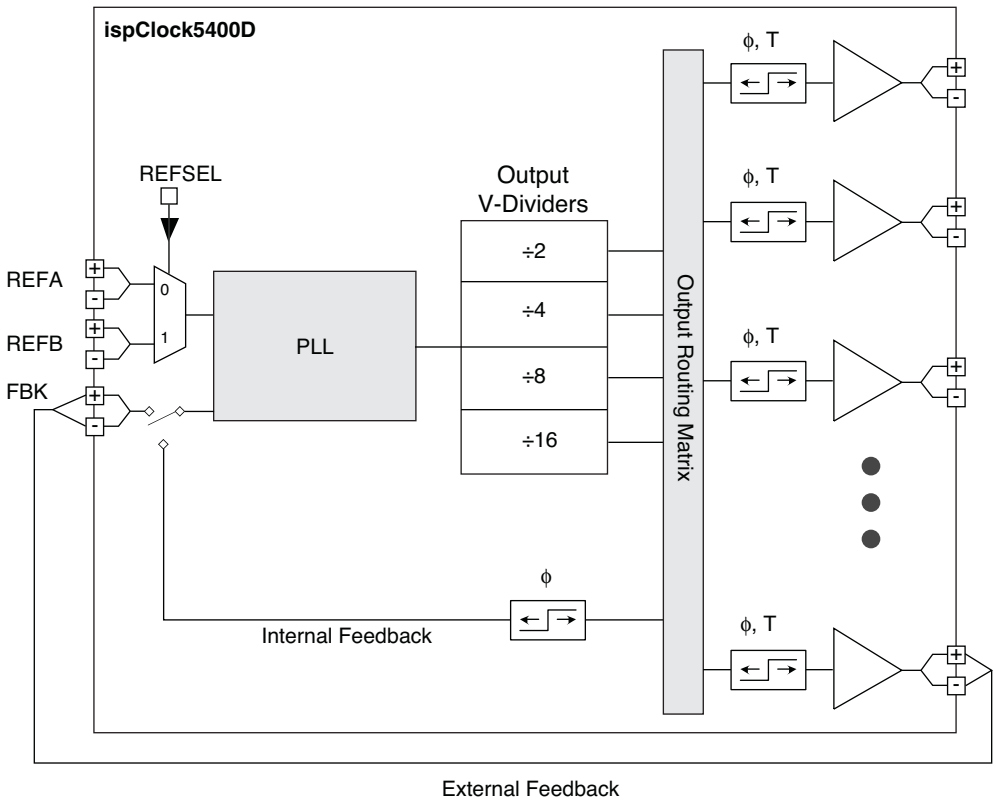
Zero Delay Buffer Mode

Figure 26 shows the ispClock5400D device configured to operate in the Zero Delay Buffer mode. The REFSEL signal is used to select the active clock from the two input reference clocks. The active input clock then drives the Phase frequency detector of the PLL. Up to four clock frequencies can be generated from the PLL clock by the use of output V-dividers. Any V-divider output can be connected to any of the Output Group.

The feedback for the PLL can be derived from any of the V-dividers using the internal feedback path. Alternatively, in applications which are sensitive to input to output delay, external feedback path can be used. In both cases, the V-divider used in the feedback path must be selected such that the PLL VCO is operating within the data sheet specified frequency range.

In this mode, both Phase and Time skew control mechanisms are active for all outputs.

Figure 26. ispClock5400D Configured as Zero Delay Buffer Mode



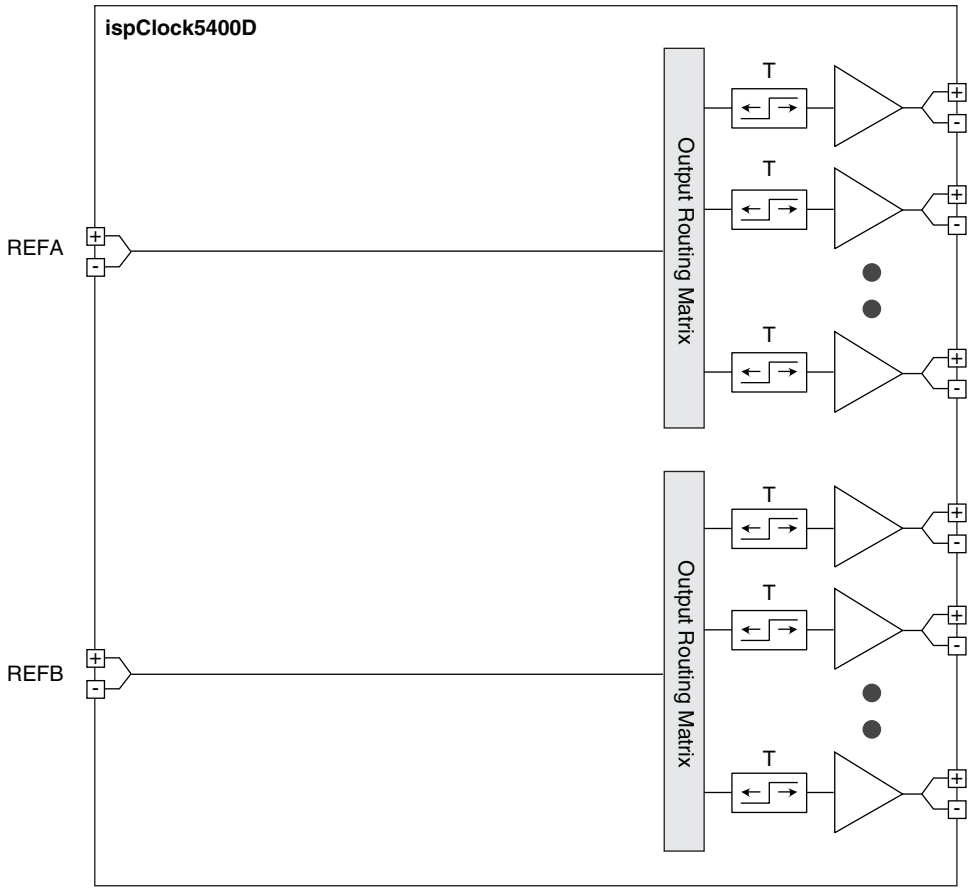
Dual Non-Zero Delay Buffer Mode (Dual Fan-Out Buffer Mode)

Figure 27 shows the operation of ispClock5400D configured in the Dual Non-Zero Delay Buffer mode. In this mode the reference clock inputs are directly routed to outputs through the output routing matrix. There is no limit to the number of Output Groups associated with either REFA or REFB.

The output skew of each clock can be independently adjusted using the Time Skew Control only. (The Phase Skew Control mechanism is not available).

Note that in Fan-out Buffer mode the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in Fan-out Buffer mode.

Figure 27. Dual Non-Zero Delay Buffer Mode



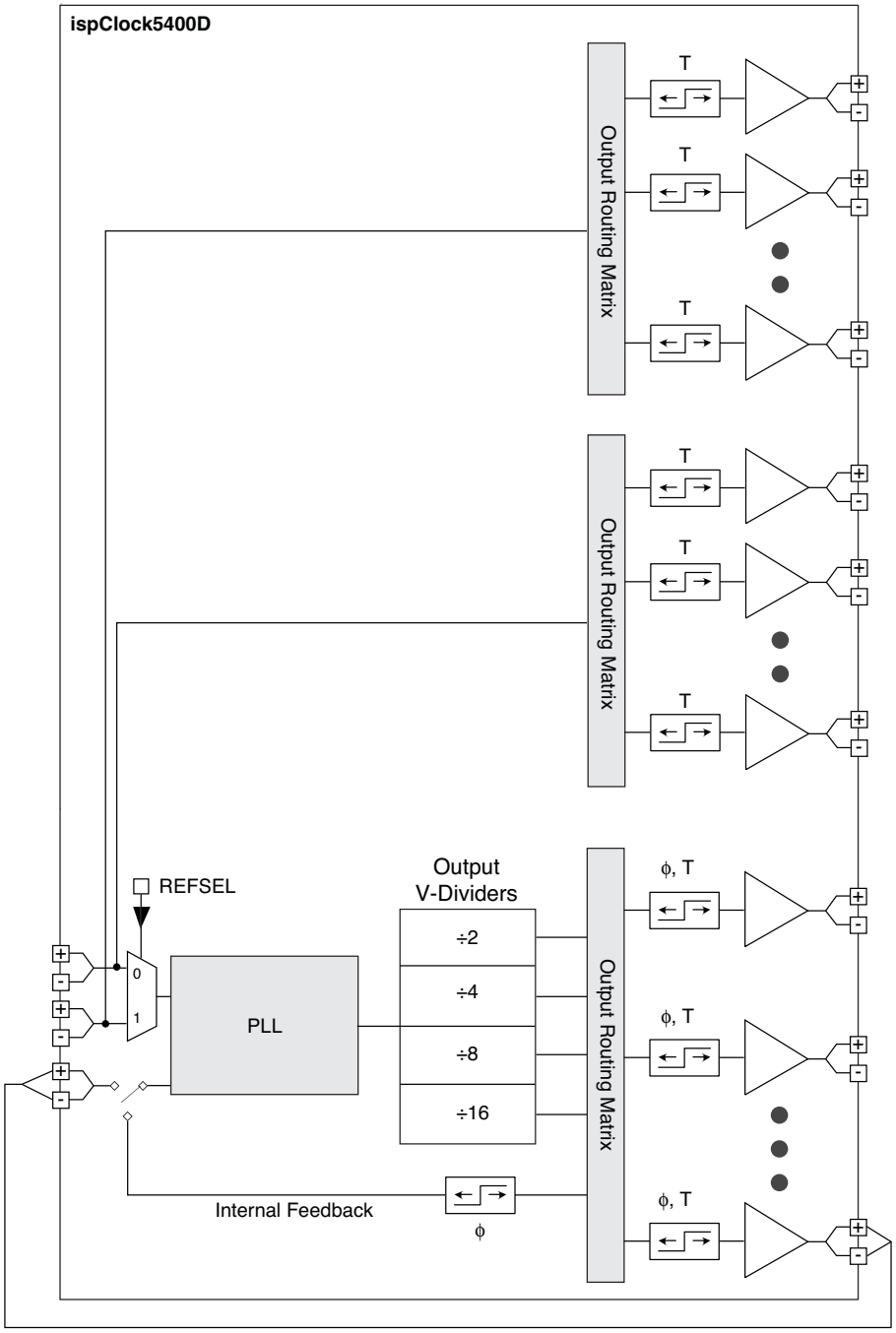
Mixed Zero Delay and Non-Zero Delay (Fan-out) Buffer Mode

Figure 28 shows the operation of the ispClock5400D in Mixed Zero Delay and Non Zero Delay modes. In this mode the output switch matrix is configured to route either of the reference clocks directly to two sets of Output Groups, and a zero delay clock through the PLL and V-dividers to the remaining Output Groups.

The Time Skew Control mechanism is available only to outputs directly connected to REFA or REFB. However, both the Phase and Time Skew Control mechanisms are available to clocks connected to V-dividers.

Note that in Fan-out Buffer mode the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in Fan-out Buffer mode.

Figure 28. Mixed Zero Delay and Non Zero Delay (Fan-out) Buffer Mode



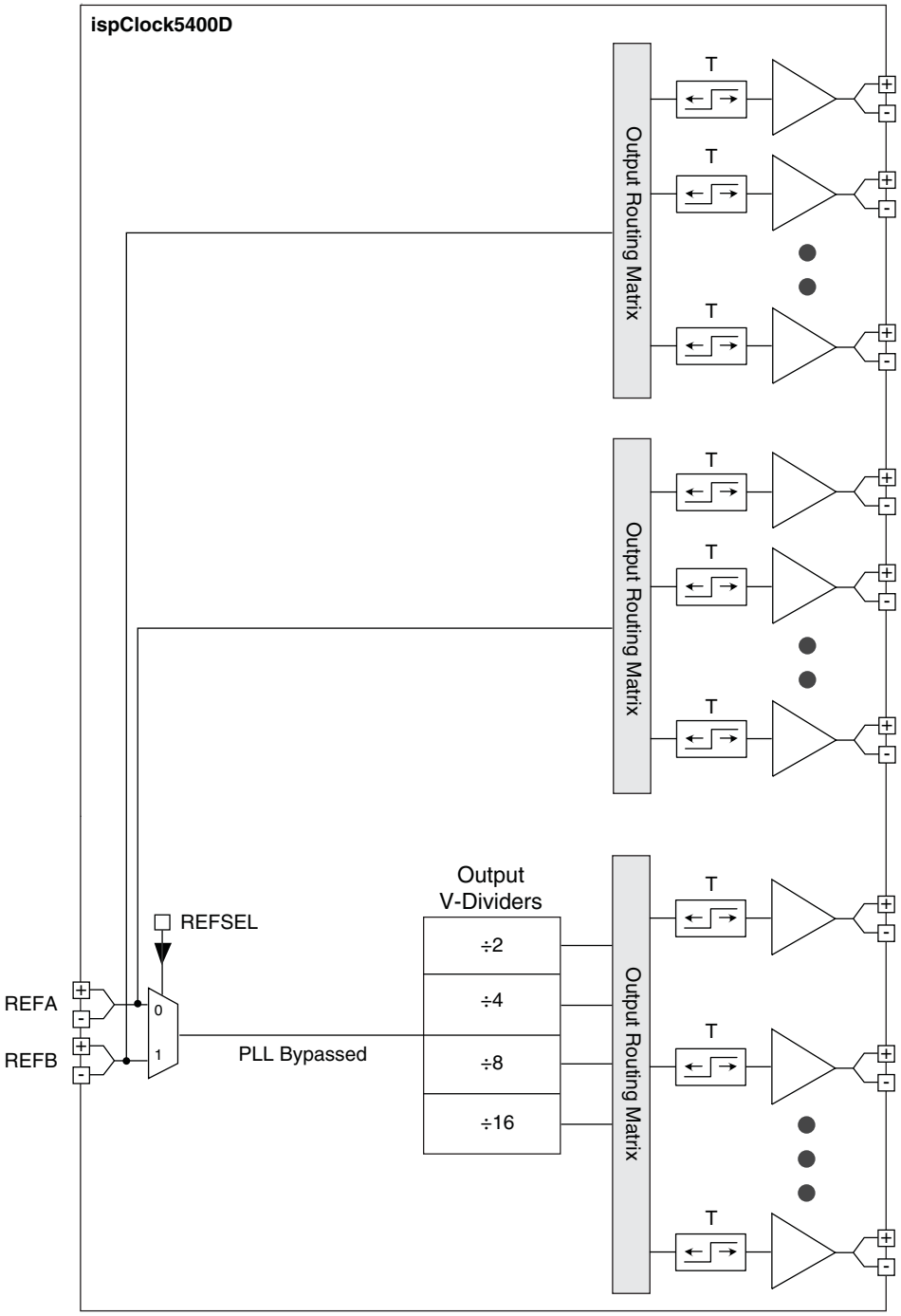
Non-Zero Delay Buffer Mode With and Without Output Clock Dividers

In the Non-Zero Delay Buffer mode shown in Figure 29 the Output Routing Matrix completely bypasses the PLL. Each of the single-ended input reference clocks can be routed to any number of available output clocks.

In this mode of operation only the Time Skew Control mechanism is available to all outputs.

Note that in the Non-Zero Delay Buffer mode without output clock dividers, the clock outputs match the input frequency and duty cycle. Reset does not disable outputs that are in the Non-Zero Delay Buffer mode when not using output clock dividers.

Figure 29. Non-Zero Delay Fan-out Buffer Mode With and Without Output Clock Division



ispClock5400D Operating Configuration Summary

Table 3 summarizes the operating modes of the ispClock5400D.

Table 3. ispClock5400D Operating Modes

ispClock5400D Operating Mode	Time Skew Control	Phase Skew Control	Output Clock Frequency Divider
Zero Delay Buffer Mode	Yes	Yes	Yes
Mixed Zero-Delay & Non-Zero Delay Buffer Mode	Yes	Only to Zero Delay Output Clocks	Only to Zero Delay Output Clocks
Dual Non-Zero Delay Fan-out Buffer Mode	Yes	No	No
Non-Zero Delay Fan-out Buffer Mode With and Without Output Clock Dividers	Yes	No	Only to Clocks Sourced From Bypassed PLL

Thermal Management

In applications where a majority of the ispClock5400D's outputs are active and operating at or near maximum output frequency, package thermal limitations may need to be considered to ensure absolute maximum junction temperature is not exceeded. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the Thermal Management document.

The maximum current consumption of the digital and analog core circuitry for ispClock5406D is 148.2mA worst case (I_{CCD} + I_{CCA} + 6 x $I_{CCADDER}$), and each of the output banks may draw up to 22mA worst case (LVPECL, CL=5pF, f_{OUT}=100 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.60V \times (6 \times 22mA + 148.2mA) = 1.01W \quad (3)$$

With an absolute maximum junction temperature (limit) of 125°C, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

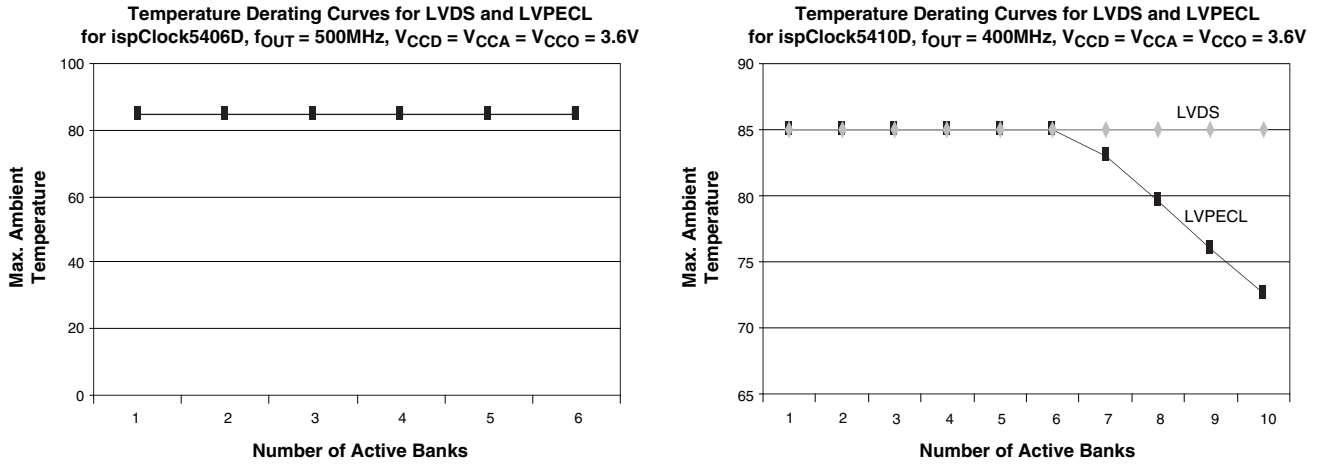
$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 125°C - 1.01W \times 39.2°C/W = 85°C \quad (4)$$

where Θ_{JA} = 39.2°C/W for the 48 QFNS package in still air and Θ_{JA} = 38.4°C/W for the 64 QFNS package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 28.6°C/W for the 48 QFNS package and 26.7°C/W for the 64 QFNS package.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 30 which shows the maximum ambient temperature permitted when operating a given number of output banks at the maximum output frequency.

Figure 30. Maximum Ambient Temperature vs. Number of Active Output Banks



Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Other Features

$\overline{\text{RESET}}$ and Power-up Functions

To ensure proper PLL startup and synchronization of outputs, the ispClock5400D provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic LOW at the $\overline{\text{RESET}}$ pin. Asserting $\overline{\text{RESET}}$ resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping.

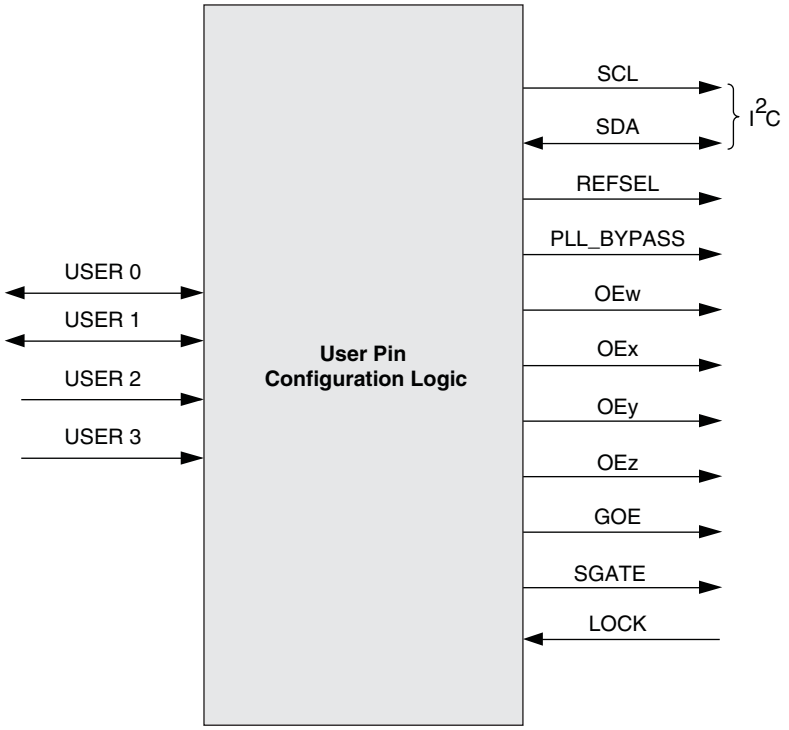
If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

USER [0..3] Pins

The ispClock5400D provides a set of four user configurable pins, USER[0..3], which can be configured to control different aspects of the device through external hardware logic. Figure 31 shows all the control functions which can be allocated to USER pins. Each of these USER pins can independently be configured as Active low/ Active high with internal pull-up/pull-down resistors. The USER 0 and USER 1 pins support both input and output while USER2 and USER3 only support input.

The configuration logic allocation is stored in the on-chip non-volatile E^2CMOS configuration.

Figure 31. ispClock5400D USER[0..3] Pins Configuration



Control/Status Signals That Can be Allocated to USER[0..3] Pins

Each of these control signals, with the exception of SGATE signal can be controlled by the I²C interface or it can be programmed to logic '0' or Logic '1' in from the on-chip, non-volatile E²CMOS configuration.

I²C Interface (SCL, SDA)

The SCL and SDA signals must be assigned to the USER pins in order to control the ispClock5400D device through the I²C interface. Note when I²C is enabled, SCL is connected to USER2 and SDA is connected to USER1 pins.

The details of control functions which can be accessed through the I²C interface are discussed in the I²C Interface section.

REFSEL

The REFSEL signal is used to select the active clock from the two reference clock inputs, REFA and REFB.

Control Signal	Logic State	Output
REFSEL (Active High)	0	REFA Input Selected for PLL
	1	REFB Input Selected for PLL

PLL_BYPASS

The on-chip PLL of the ispClock5400D device can be bypassed by using the PLL_BYPASS signal. If the PLL_BYPASS signal is not routed to the USER pins, it can be controlled by I²C interface only if the PLL_BYPASS bit is programmed as Logic 1 in the on-chip, non-volatile E²CMOS configuration.

Control Signal	Logic State	Output
PLL_Bypass (Active High)	0	PLL Bypassed
	1	PLL Active

OEw, OEx, OEy, OEz, GOE

The ispClock5400D family provides five output control pins for enabling and disabling clock outputs. Any of the OE[w..z] signals can be allocated to control any number of output pins. In addition, the GOE signal disables all the outputs. Note that the OE is an asynchronous signal and it can cause runt clock pulses.

Control Signal	Logic State	Output
OEw, OEx, OEy, OEz, GOE (Active High)	0	Output Active
	1	Output Tristate

SGATE

The SGATE (Synchronous Gate Control) signal turns the clock on or off without generating runt clock pulses. The internal synchronization logic ensures that the output controlled by the SGATE signal completes the clock cycle before settling at logic '0' or logic '1' depending on the output clock invert configuration. Any output can be controlled by the SGATE signal. Because the SGATE signal cannot be controlled by the I^2C interface, this signal should be routed to USER pins if this feature is required.

Control Signal	Logic State	Output
SGATE (Active High)	0	Output Not Controlled by SGATE
	1	Output Disabled By SGATE

LOCK

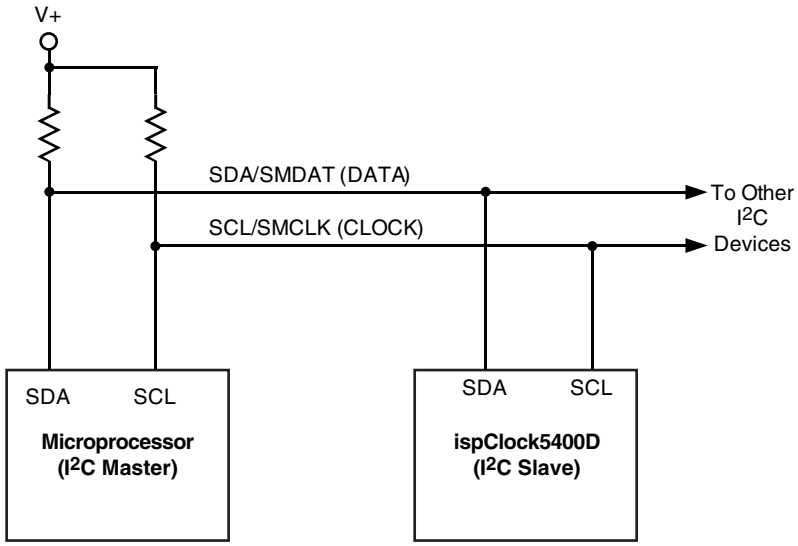
This is the only status signal which can be routed to the USER pins. The lock-detection feature is associated with the PFD in the PLL. When the ispClock5400D is in a LOCKED state, the LOCK output pin goes HIGH or LOW depending on the configuration. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256. Note that the LOCK signal can be allocated only to the USER 0 pin.

I^2C/SMBus Interface

I^2C and SMBus are low-speed serial interface protocols designed to enable communications among a number of devices on a circuit board. The ispClock5400D supports a 7-bit addressing of the I^2C communications protocol. Figure 32 shows a typical I^2C configuration, in which one or more ispClock5400D devices are slaved to a microcontroller. SDA is used to carry data signals, while SCL provides a synchronous clock signal. The 7-bit I^2C address of the ispClock5400D is fully programmable through the JTAG port.

In both the I^2C and SMBus protocols, the bus is controlled by a single MASTER device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The ispClock5400D is configured as a slave device and cannot independently coordinate data transfers.

Figure 32. ispClock5400D in an I²C/SMBus System



Each slave device on a given I²C bus is assigned a unique address. The ispClock5400D implements the 7-bit addressing portion of the standard. Any 7-bit address can be assigned to the ispClock5400D device by programming through JTAG. When selecting a device address, note that several addresses are reserved by the I²C and/or SMBus standards, and should not be assigned to ispClock5400D devices to assure bus compatibility. Table 4 lists these reserved addresses.

Table 4. I²C/SMBus Reserved Slave Device Addresses

Address	R/W	I²C Function	SMBus Function
0000 000	0	General Call Address	General Call Address
0000 000	1	Start Byte	Start Byte
0000 001	x	CBUS Address	CBUS Address
0000 010	x	Reserved	Reserved
0000 011	x	Reserved	Reserved
0000 1xx	x	HS Mode Master Code	HS Mode Master Code
0001 000	x	N/A	SMBus Host
0001 100	x	N/A	SMBus Alert Response Alert Response Address
0101 000	x	N/A	Reserved for ACCESS.bus
0110 111	x	N/A	Reserved for ACCESS.bus
1100 001	x	N/A	SMBus Device Default Address
1111 0xx	x	10-Bit Addressing	10-Bit Addressing
1111 1xx	x	Reserved	Reserved

The ispClock5400D's I²C/SMBus interface allows data to be both written to and read from the device. A data write transaction (Figure 33) consists of the following operations:

1. Start the bus transaction

2. Transmit the device address (7 bits) along with a low write bit

3. Transmit the address of the register to be written to (8 bits)

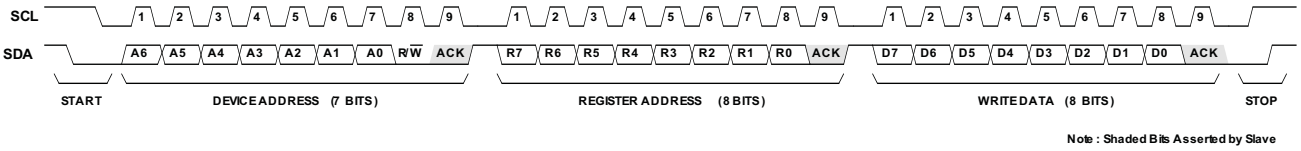
4. Transmit the data to be written (8 bits)

5. Stop the bus transaction

To start the transaction, the master device holds the SCL line high while pulling SDA low. Address and data bits are then transferred on each successive SCL pulse, in three consecutive byte frames of nine SCL pulses. Address and data are transferred on the first eight SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the ninth clock in each frame. Both data and addresses are transferred in a most-significant-bit-first format.

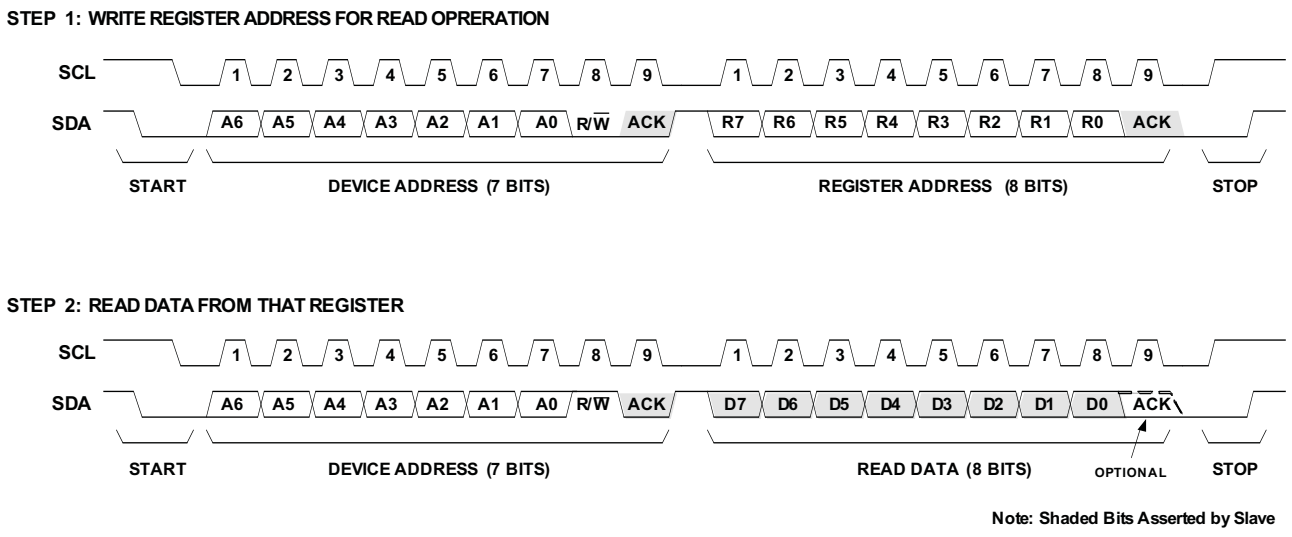
The first frame contains the 7-bit device address, with bit 8 held low to indicate a write operation. The second frame contains the register address to which data will be written, and the final frame contains the actual data to be written. Note that the SDA signal is only allowed to change when the SCL is low, as raising SDA when SCK is high signals the end of the transaction.

Figure 33. I²C Write Operation



Reading a data byte from the ispClock5400D requires two separate bus transactions (Figure 34). The first transaction writes the register address from which a data byte is to be read. Note that since no data is being written to the device, the transaction is concluded after the second byte frame. The second transaction performs the actual read. The first frame contains the 7-bit device address with the R/W bit held High. In the second frame the ispClock5400D asserts data out on the bus in response to the SCK signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the ispClock5400D.

Figure 34. I²C Read Operation



The ispClock5400D provides 28 registers that can be accessed through its I²C interface. These registers provide the user with the ability to control most of the programmable features of the device. Table 6 provides a summary of these registers.

Table 5. Summary of ispClock5406D I²C Registers

Hex Address	I²C R/W	Value After POR[1]	Bit Assignment								Description
			7	6	5	4	3	2	1	0	
00	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_0 Control
01	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_1 Control
02	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
03	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
04	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_2 Control
05	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_3 Control
06	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
07	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
08	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_4 Control
09	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_5 Control
0A	RW	E²CMOS	0	EN-I-FBK	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Internal Feedback Control
0B		N/A	0	0	0	0	0	0	0	0	Reserved
0C		N/A	0	0	0	0	0	0	0	0	Reserved
0D	RW	E²CMOS	T-SKEW_1-3	T-SKEW_1-2	T-SKEW_1-1	T-SKEW_1-0	T-SKEW_0-3	T-SKEW_0-2	T-SKEW_0-1	T-SKEW_0-0	Output Group 0 Time Skew
0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
0F	RW	E²CMOS	T-SKEW_5-3	T-SKEW_5-2	T-SKEW_5-1	T-SKEW_5-0	T-SKEW_4-3	T-SKEW_4-2	T-SKEW_4-1	T-SKEW_4-0	Output Group 1 Time Skew
10	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
11	RW	E²CMOS	T-SKEW_9-3	T-SKEW_9-2	T-SKEW_9-1	T-SKEW_9-0	T-SKEW_8-3	T-SKEW_8-2	T-SKEW_8-1	T-SKEW_8-0	Output Group 2 Time Skew
12	RW	E²CMOS	EN-T-SKEW_5	EN-T-SKEW_4	0	0	EN-T-SKEW_3	0	0	0	Time Skew Mechanism Enable
13	RW	E²CMOS	EN-T-SKEW_2	0	0	EN-T-SKEW_1	EN-T-SKEW_0	0	0	0	Time Skew Mechanism Enable
14	RW	E²CMOS	0	0	0	0	0	0	REFSEL	PLL_BYPASS	PLL Control
15	RW	E²CMOS	FOB-BANK_5	FOB-BANK_4	0	0	FOB-BANK_3	0	0	0	FAN OUT Buffer Selection
16	RW	E²CMOS	FOB-BANK_2	0	0	FOB-BANK_1	FOB-BANK_0	0	0	0	FAN OUT Buffer Selection
17	RW	E²CMOS	FOB-REFSEL_45	0	FOB-REFSEL_23	0	FOB-REFSEL_01	0	0	0	FOB Reference Clock/Output Group
18	W	E²CMOS	1	0	1	1	0	1	0	0	Safe State
19	W	E²CMOS	0	1	0	1	1	0	1	0	Soft Reset
1A	W	E²CMOS	1	1	1	0	1	0	0	1	Full Reset
1B	R	E²CMOS	$\overline{UES07}$	$\overline{UES06}$	$\overline{UES05}$	$\overline{UES04}$	$\overline{UES03}$	$\overline{UES02}$	$\overline{UES01}$	$\overline{UES00}$	UES Byte 0[2]
1C	R	E²CMOS	$\overline{UES15}$	$\overline{UES14}$	$\overline{UES13}$	$\overline{UES12}$	$\overline{UES11}$	$\overline{UES10}$	$\overline{UES09}$	$\overline{UES08}$	UES Byte 1[2]
1D	R	E²CMOS	$\overline{UES23}$	$\overline{UES22}$	$\overline{UES21}$	$\overline{UES20}$	$\overline{UES19}$	$\overline{UES18}$	$\overline{UES17}$	$\overline{UES16}$	UES Byte 2[2]
1E	R	E²CMOS	$\overline{UES31}$	$\overline{UES30}$	$\overline{UES29}$	$\overline{UES28}$	$\overline{UES27}$	$\overline{UES26}$	$\overline{UES25}$	$\overline{UES24}$	UES Byte 3[2]
1F		N/A	0	0	0	0	0	0	0	0	Reserved
20		N/A	0	0	0	0	0	0	0	0	Reserved

1. OE data is not associated with E²CMOS. Bits are 0 after POR.
2. UES register bits are inverted.

Table 6. Summary of ispClock5410D I²C Registers

Hex Address	I²C R/W	Value After POR[1]	Bit Assignment								Description
			7	6	5	4	3	2	1	0	
00	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_0 Control
01	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 0, BANK_1 Control
02	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_2 Control
03	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 1, BANK_3 Control
04	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_4 Control
05	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 2, BANK_5 Control
06	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 3, BANK_6 Control
07	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 3, BANK_7 Control
08	RW	E²CMOS	INVERT	OE	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 4, BANK_8 Control
09	RW	E²CMOS	INVERT	OE	1	1	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Output Group 4, BANK_9 Control
0A	RW	E²CMOS	0	EN-I-FBK	FREQ-SEL1	FREQ-SEL0	P-SKEW3	P-SKEW2	P-SKEW1	P-SKEW0	Internal Feedback Control
0B		N/A	0	0	0	0	0	0	0	0	Reserved
0C		N/A	0	0	0	0	0	0	0	0	Reserved
0D	RW	E²CMOS	T-SKEW_1-3	T-SKEW_1-2	T-SKEW_1-1	T-SKEW_1-0	T-SKEW_0-3	T-SKEW_0-2	T-SKEW_0-1	T-SKEW_0-0	Output Group 0 Time Skew
0E	RW	E²CMOS	T-SKEW_3-3	T-SKEW_3-2	T-SKEW_3-1	T-SKEW_3-0	T-SKEW_2-3	T-SKEW_2-2	T-SKEW_2-1	T-SKEW_2-0	Output Group 1 Time Skew
0F	RW	E²CMOS	T-SKEW_5-3	T-SKEW_5-2	T-SKEW_5-1	T-SKEW_5-0	T-SKEW_4-3	T-SKEW_4-2	T-SKEW_4-1	T-SKEW_4-0	Output Group 2 Time Skew
10	RW	E²CMOS	T-SKEW_7-3	T-SKEW_7-2	T-SKEW_7-1	T-SKEW_7-0	T-SKEW_6-3	T-SKEW_6-2	T-SKEW_6-1	T-SKEW_6-0	Output Group 3 Time Skew
11	RW	E²CMOS	T-SKEW_9-3	T-SKEW_9-2	T-SKEW_9-1	T-SKEW_9-0	T-SKEW_8-3	T-SKEW_8-2	T-SKEW_8-1	T-SKEW_8-0	Output Group 5 Time Skew
12	RW	E²CMOS	EN-T-SKEW_9	EN-T-SKEW_8	EN-T-SKEW_7	EN-T-SKEW_6	EN-T-SKEW_5	0	0	0	Time Skew Mechanism Enable
13	RW	E²CMOS	EN-T-SKEW_4	EN-T-SKEW_3	EN-T-SKEW_2	EN-T-SKEW_1	EN-T-SKEW_0	0	0	0	Time Skew Mechanism Enable
14	RW	E²CMOS	0	0	0	0	0	0	REFSEL	PLL_BYPASS	PLL Control
15	RW	E²CMOS	FOB-BANK_9	FOB-BANK_8	FOB-BANK_7	FOB-BANK_6	FOB-BANK_5	0	0	0	FAN OUT Buffer Selection
16	RW	E²CMOS	FOB-BANK_4	FOB-BANK_3	FOB-BANK_2	FOB-BANK_1	FOB-BANK_0	0	0	0	FAN OUT Buffer Selection
17	RW	E²CMOS	FOB-REFSEL_89	FOB-REFSEL_67	FOB-REFSEL_45	FOB-REFSEL_23	FOB-REFSEL_01	0	0	0	FOB Reference Clock/Output Group
18	W	E²CMOS	1	0	1	1	0	1	0	0	Safe State
19	W	E²CMOS	0	1	0	1	1	0	1	0	Soft Reset
1A	W	E²CMOS	1	1	1	0	1	0	0	1	Full Reset
1B	R	E²CMOS	$\overline{UES07}$	$\overline{UES06}$	$\overline{UES05}$	$\overline{UES04}$	$\overline{UES03}$	$\overline{UES02}$	$\overline{UES01}$	$\overline{UES00}$	UES Byte 0[2]
1C	R	E²CMOS	$\overline{UES15}$	$\overline{UES14}$	$\overline{UES13}$	$\overline{UES12}$	$\overline{UES11}$	$\overline{UES10}$	$\overline{UES09}$	$\overline{UES08}$	UES Byte 1[2]
1D	R	E²CMOS	$\overline{UES23}$	$\overline{UES22}$	$\overline{UES21}$	$\overline{UES20}$	$\overline{UES19}$	$\overline{UES18}$	$\overline{UES17}$	$\overline{UES16}$	UES Byte 2[2]
1E	R	E²CMOS	$\overline{UES31}$	$\overline{UES30}$	$\overline{UES29}$	$\overline{UES28}$	$\overline{UES27}$	$\overline{UES26}$	$\overline{UES25}$	$\overline{UES24}$	UES Byte 3[2]
1F		N/A	0	0	0	0	0	0	0	0	Reserved
20		N/A	0	0	0	0	0	0	0	0	Reserved

1. OE data is not associated with E²CMOS. Bits are 0 after POR.
2. UES register bits are inverted.

I²C Register Descriptions

Output Group [0..4], Bank[0..9] Control – Register Address# [00H..09H]

Two successive address locations control an Output Group. For example, addresses 00H and 01H control Output Group 0 (Bank_0 and Bank_1). The control bits are as follows:

- **INVERT** – Inverts the output clock when reset to 0.
- **OE** – When set to 1, tri-states that output if the output has been programmed to be controlled by I²C. Otherwise, this bit will be ignored. (E²CMOS or USER pin output disable has priority over I²C).
- **FREQ-SEL[1,0]** – Selects the V-divider for that Output Group (shown in the table below). The corresponding bits for the second output of that Output Group should be set to 11.

FREQ-SEL-1	FREQ-SEL-0	V-divider Selection
0	0	÷2
0	1	÷4
1	0	÷8
1	1	÷16

- **P-SKEW[3..0]** – Sets the clock phase skew for that output. The actual delay can be set from 0 to 15 Phase Delay Units.

Internal Feedback Control – Register Address# 0AH

The ispClock5400D PLL feedback can be derived either externally from the FBK pin or internally directly from the Output Routing Matrix. The control bits are as follows:

- **EN-I-FBK** – When set, enables the internal feedback path. The output clock connected to the FBK pins is ignored at that time.
- **FREQ-SEL[1,0]** – Selects the V-divider for the internal feedback clock (shown in the table below).

FREQ-SEL-1	FREQ-SEL-0	V-divider Selection
0	0	÷2
0	1	÷4
1	0	÷8
1	1	÷16

Note: Avoid exceeding maximum f_{VCO} when changing feedback V-divider setting.

- **P-SKEW[3..0]** – Sets the clock phase skew for the internal feedback clock. The actual delay can be set from 0 to 15 Phase Delay Units.

Output Group [0..4] Time Skew Control – Register Address [0DH..11H]

Each byte enables controlling of time skew of both the banks in that output group. For example, Address 0DH controls Time Skew of Bank_0 and Bank_1.

- **T-SKEW_1-[3..0]** – Sets the clock time skew for the Bank_1 clock. The actual delay can be set from 0 to 15 Time Delay Units.
- **T-SKEW_0-[3..0]** – Sets the clock time skew for the Bank_0 clock. The actual delay can be set from 0 to 15 Time Delay Units.

Enable Time Skew Control Mechanism – Register Address [12..13]

Each enable bit, when set, enables the time skew mechanism for that bank. For example, EN-TSKEW_9 bit, when set, enables the Time Skew mechanism for Bank_9 output clock. The Bank_9 output clock skew delay value are determined by T-SKEW_9-[3..0] bits at address location 11H. E²CMOS settings must be such that Time Skew is powered up for any bank for which Time Skew control is desired.

PLL Control – Register Address – 14H

This register selects the active clock routed to the PLL as well as the PLL bypass control.

- **REFSEL** – REFA input clock gets routed to the PLL when this bit is reset to 0 and when set, the REFB input clock will be routed to PLL.
- **PLL_BYPASS** – When reset to 0, bypasses the PLL and deactivates the Phase Skew Control mechanism for all banks. The P-SKEW[3..0] setting will be ignored. However, the T-Skew mechanism can still be activated on a bank-by bank basis.E^2CMOS settings must be such that PLL mode is enabled. E^2CMOS and USER pin control of PLL bypass overrides I^2C control.

Fan-out Buffer (FOB) Selection – Register Address# – [15H..16H]

The Output Routing Matrix connects a clock from either the PLL or directly from either of the reference clocks to an Output Group. The two banks in that Output Group can then be individually configured to output either the clock from the PLL or from the Reference clock using these bits.

For example, the Bank_2 will output Reference clock when FOB-BANK_2 bit is set at register 16.

- **FOB_Bank_[9..0]** – When set, outputs the Reference clock connected to that Output Group.

FOB Reference Clock per Output Group Selection – Register Address# – 17H

Any output group can receive the clock either from the PLL or from the input reference clock. The FOB-REFSEL_01..FOB-REFSEL_04 bits enable the selection between the REFA and REFB clocks. For example, FOB-REFSEL_23 bit, when set, enables REFB clock to Output Group 1 and when reset to 0, enables REFA clock to Output Group 1.

Safe State - Register Address# – 18H, Followed by Data Byte Value = B4H

After a value of B4H is written into the Address location 18H, the ispClock5400D enters the safe state. During this state, all clock outputs are tri-stated. One can use this instruction to stop the output clocks before updating the I^2C registers. Writing a code other than B4H into the same location brings the device back out of the safe state mode; all the clocks will be operational. Safe State tristates all outputs including those that are in Fan-out Buffer mode.

Note: The activation of safe state can result in runt clock output. If runt clocks are not desired, one should disable the clock using the SGATE feature, before entering the safe state.

Soft Reset – Register Address# – 19H, Followed by Data Byte Value = 5AH

The ispClock5400D device enters the Soft Reset state as soon as the 5AH is written into the address location 19H. During this state the PLL, Dividers, Phase and Time Skew blocks are reset. The actual configuration is not changed. Writing a value other than 5AH into address location 19H brings ispClock5400D device out of the soft reset mode and all outputs begin to output clocks with delays as configured. During Soft Reset, differential outputs are low. Note that Soft Reset does not affect outputs that are in Fan-out Buffer mode.

Full Reset - Register Address# – 1AH, Followed by Data Byte Value = E9H

The ispClock5400D device enters full reset state as soon as a value of E9H is written into address location of 1AH. During this state, all configuration registers are updated from the E^2CMOS configuration. All the values loaded by I^2C will be overwritten. This command is equivalent to toggling the RESETb pin of the ispClock5400D device. Writing a value other than E9H to the same location will bring the device out of Full Reset. During Full Reset, differential outputs are low. Note that Full Reset does not affect the outputs that are in Fan-out Buffer mode.

User Electronic Signature (UES) - Register Address# – [1BH..1EH]

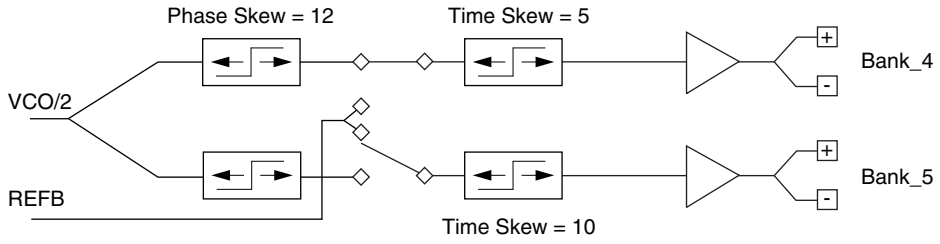
Using the I^2C interface, one can read all 32 bits of programmed UES bits from the locations 1BH to 1FH. Note: These four locations are read only and each of the UES bits is inverted.

Example

The following describes Output Group 2 (Bank_4 and Bank_5) configuration. Refer to Figure 35.

- Bank_4 output Non-inverted clock received from V-divider ÷2 (Frequency = VCO Clock/2)
- Bank_5 output Inverted clock Received from REFB
- Phase Skew for Bank_4 output clock set to 12 PUD
- Time Skew for Bank_4 output clock set to 5 TUD
- It is not possible to set Phase Skew for Bank_5 because it does not derive clock from PLL The Phase Skew value set in the register will be ignored.
- Time Skew for Bank_5 output clock set to 10 TUD
- All other banks are not used

Figure 35. Example Configuration of ispClock5410D Output Group 2



The I^2C Register Bit values for this configuration are as follows:

Register Address# 04H (Output Group 2, Bank_4 Output Control) = '1000 1100' B
INVERT = 1, OE = 0, FREQ_SEL[1..0] = 00B (0), P-SKEW[3..0] = 1100B (12)

Register Address# 05H (Output Group 2,Bank_5 Output Control) = '0011 0000' B
INVERT = 0, OE = 0, FREQ_SEL[1..0] = 11B, P-SKEW[3..0] = 0000B (0)

Register Address# 0FH (Output Group 2 Time Skew) = '1010 0101B'
T-SKEW_4-[3..0] = 0101B (5 TUD), T-SKEW_5-[3..0] = 1010B (10 TUD)

Register Address# 12H (Time Skew Mechanism Enable) = '0000 1000'B
EN-TSKEW_5 = 1 (T-Skew mechanisms for Banks 6 to 9 have been turned off)

Register Address# 13H (Time Skew Mechanism Enable) = '1000 0000'B
EN-TSKEW_4 = 1 (T-Skew mechanisms for Banks 0 to 3 have been turned off)

Register Address# 15H (Fan out Buffer Selection) = '0000 1000'B
FOB-BANK_5 = 1, (BANK_6 to BANK_9 are connected to V-dividers)

Register Address# 16H (Fan out Buffer Selection) = '0000 0000'B
(BANK_0 to BANK_4 are connected to V-dividers)

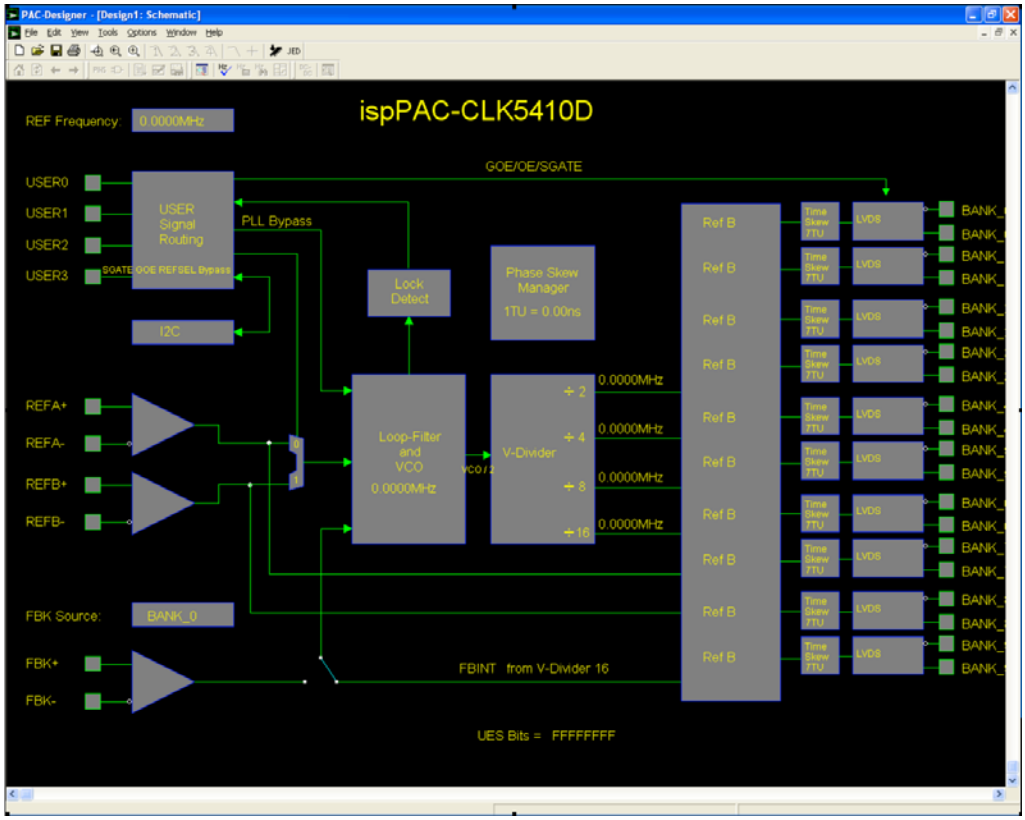
Register Address# 17H (FOB Reference clock per Output Group) = '0010 0000'B
FOB-REFSEL_54 = 1, (REFB Clock is selected for BANK_5 and BANK_4)

Software-Based Design Environment

Designers can configure the ispClock5400D using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5400D. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. PAC-Designer is available for

download from the Lattice web site. The PAC-Designer schematic window, shown in Figure 36 provides access to all configurable ispClock5400D elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 36. PAC-Designer Design Entry Screen



In-System Programming

The ispClock5400D is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^2CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^2CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5400D instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^2CMOS memory of the ispClock5400D. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5400D device to prevent unauthorized readout of the E^2CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

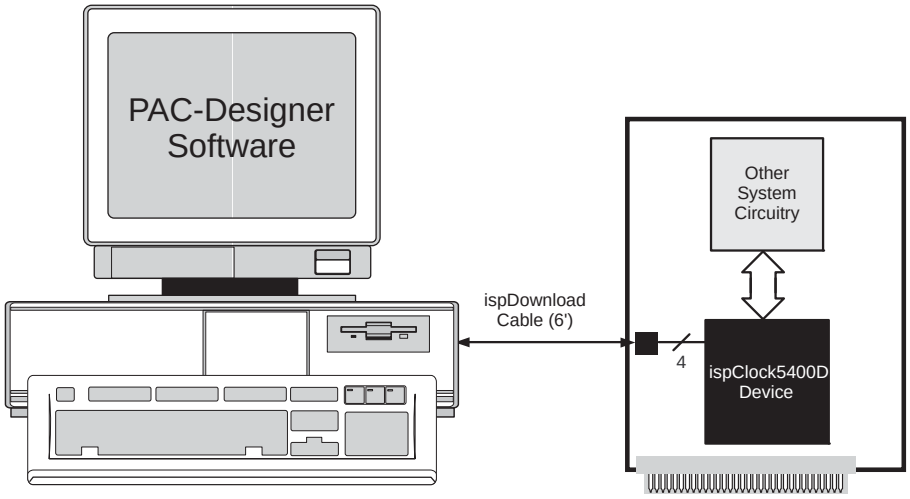
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user's specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5400D Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5400D and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5400D for a given application. (Figure 37).

Part Number	Description
PACCLK5406D-P-EVN	Complete system kit, evaluation board, ispDOWNLOAD cable and software.

Figure 37. Download from a PC



IEEE Standard 1149.1 Interface (JTAG)

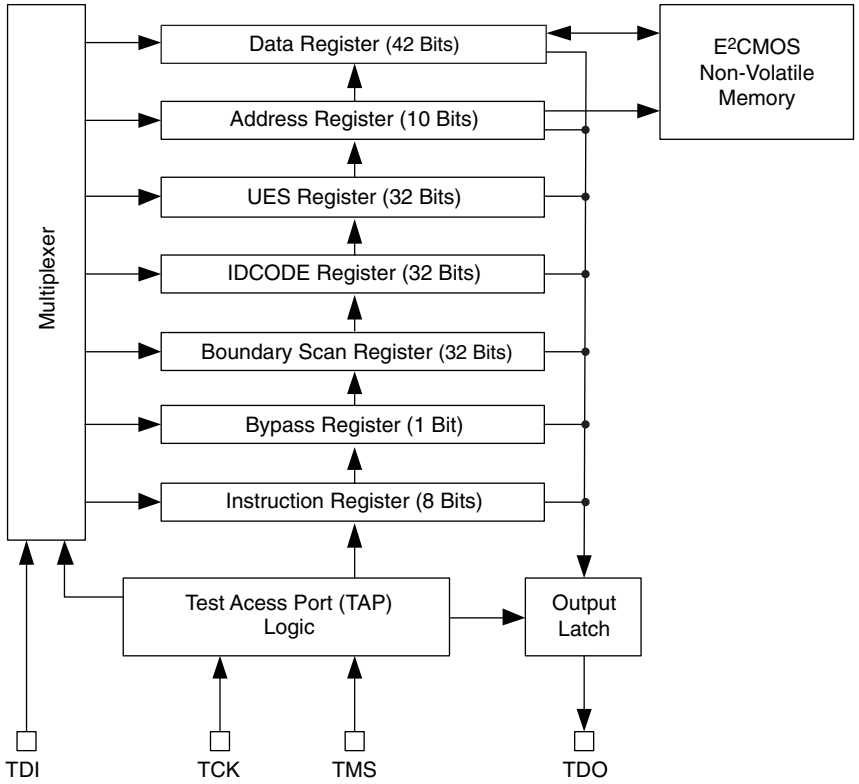
Serial Port Programming Interface Communication with the ispClock5400D is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5400D both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5400D JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5400D. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration of the ispClock5400D. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 38 shows how the

instruction and various data registers are organized in an ispClock5400D.

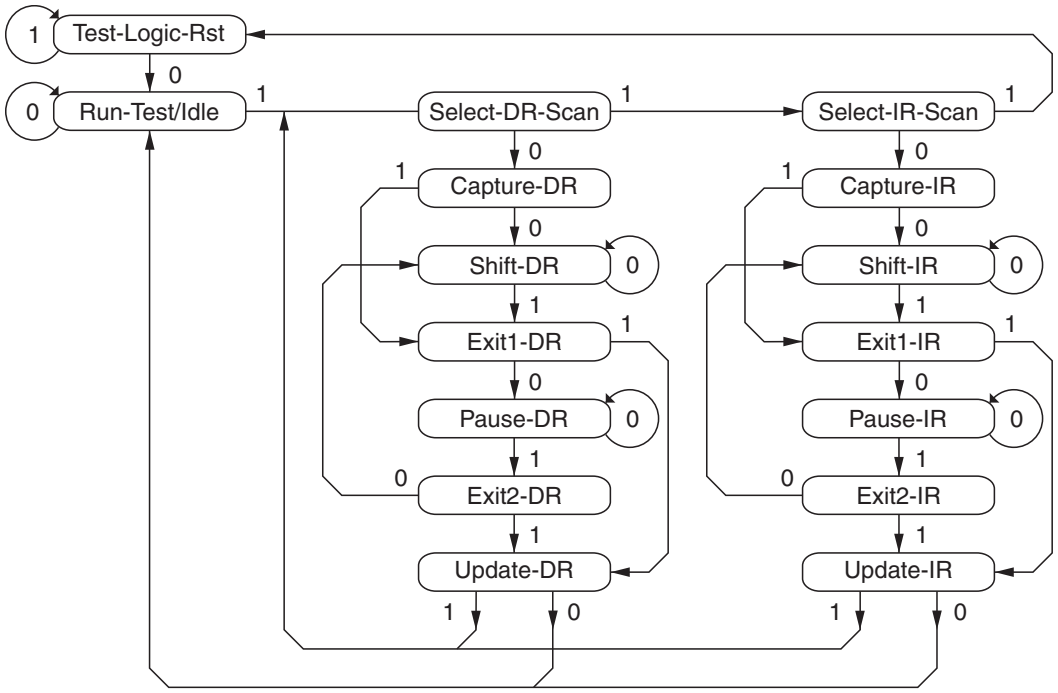
Figure 38. ispClock5400D TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 39. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run- Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 39. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5400D contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified. For ispClock5400D, the instruction word length is eight bits. All ispClock5400D instructions available to users are

shown in Table 7.

The following table lists the instructions supported by the ispClock5400D JTAG Test Access Port (TAP) controller:

Table 7. ispClock5400D TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (42 bits for ispClock5410D and 5406D)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

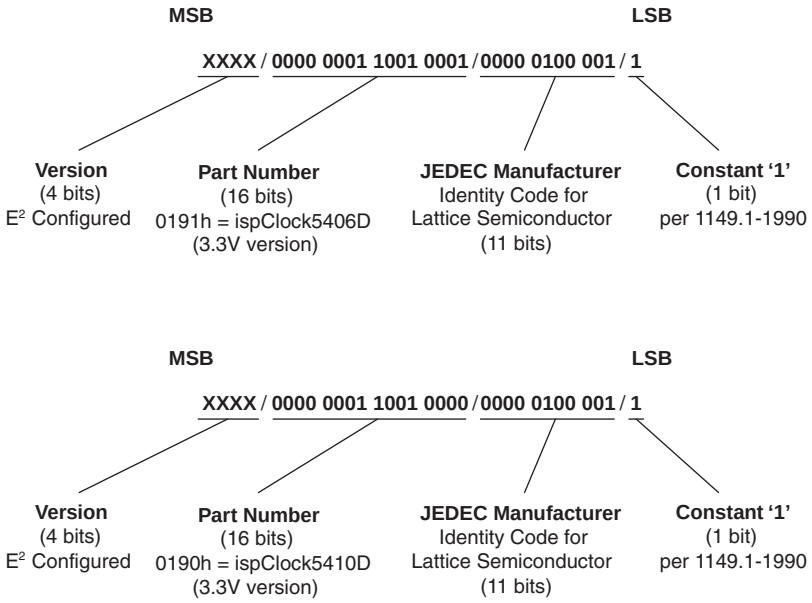
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5400D. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 7.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5400D and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 40). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 7.

Figure 40. ispClock5400D Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5400D. These instructions are primarily used to interface to the various user registers and the E^{2}CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 7.

PROGRAM_ENABLE – This instruction enables the ispClock5400D programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5400D programming mode.

BULK_ERASE – This instruction will erase all E^{2}CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (43 bits), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^{2}CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^{2}CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^{2}CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5400D for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the ‘DONE’ bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the ‘DONE’ bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions – ispClock5410D, 5406D

Pin Name	Description	Pin Type	Pin Number	
			ispClock5410D 64-Pin QFNS	ispClock5406D 48-Pin QFNS
VCCO_0	VCC For BANK_0 Output Driver	Power	46	33
VCCO_1	VCC For BANK_1 Output Driver	Power	45	32
VCCO_2	VCC For BANK_2 Output Driver	Power	39	25
VCCO_3	VCC For BANK_3 Output Driver	Power	38	12
VCCO_4	VCC For BANK_4 Output Driver	Power	32	5
VCCO_5	VCC For BANK_5 Output Driver	Power	17	4
VCCO_6	VCC For BANK_6 Output Driver	Power	11	
VCCO_7	VCC For BANK_7 Output Driver	Power	10	
VCCO_8	VCC For BANK_8 Output Driver	Power	4	
VCCO_9	VCC For BANK_9 Output Driver	Power	3	
GNDO_0	GND For BANK_0 Output Driver	GND	49	36
GNDO_1	GND For BANK_1 Output Driver	GND	42	29
GNDO_2	GND For BANK_2 Output Driver	GND		28
GNDO_3	GND For BANK_3 Output Driver	GND	35	9
GNDO_4	GND For BANK_4 Output Driver	GND		8
GNDO_5	GND For BANK_5 Output Driver	GND	14	1
GNDO_6	GND For BANK_6 Output Driver	GND		
GNDO_7	GND For BANK_7 Output Driver	GND	7	
GNDO_8	GND For BANK_8 Output Driver	GND		
GNDO_9	GND For BANK_9 Output Driver	GND	64	
BANK_0P	Bank_0 Clock Output Driver Positive	Output	48	35
BANK_0N	Bank_0 Clock Output Driver Negative	Output	47	34
BANK_1P	Bank_1 Clock Output Driver Positive	Output	44	31
BANK_1N	Bank_1 Clock Output Driver Negative	Output	43	30
BANK_2P	Bank_2 Clock Output Driver Positive	Output	41	27
BANK_2N	Bank_2 Clock Output Driver Negative	Output	40	26
BANK_3P	Bank_3 Clock Output Driver Positive	Output	37	10
BANK_3N	Bank_3 Clock Output Driver Negative	Output	36	11
BANK_4P	Bank_4 Clock Output Driver Positive	Output	34	6
BANK_4N	Bank_4 Clock Output Driver Negative	Output	33	7
BANK_5P	Bank_5 Clock Output Driver Positive	Output	15	2
BANK_5N	Bank_5 Clock Output Driver Negative	Output	16	3
BANK_6P	Bank_6 Clock Output Driver Positive	Output	12	
BANK_6N	Bank_6 Clock Output Driver Negative	Output	13	
BANK_7P	Bank_7 Clock Output Driver Positive	Output	8	
BANK_7N	Bank_7 Clock Output Driver Negative	Output	9	
BANK_8P	Bank_8 Clock Output Driver Positive	Output	5	
BANK_8N	Bank_8 Clock Output Driver Negative	Output	6	
BANK_9P	Bank_9 Clock Output Driver Positive	Output	1	
BANK_9N	Bank_9 Clock Output Driver Negative	Output	2	
VCCA	Analog VCC for the PLL Circuitry	Power	28,30	23
GNDA	Analog GND for the PLL Circuitry	GND	18	13

Pin Descriptions – ispClock5410D, 5406D (Continued)

Pin Name	Description	Pin Type	Pin Number	
			ispClock5410D 64-Pin QFNS	ispClock5406D 48-Pin QFNS
VCCD	Digital Core VCC	Power	57,59	44
GNDD	Digital GND	GND	56	43
RREF	HCSL Reference Resistor Connection Pin	REF	31	24
REFAP	Clock Input Reference A, Positive	Input	21	16
REFAN	Clock Input Reference A, Negative	Input	20	15
REFBP	Clock Input Reference B, Positive	Input	24	19
REFBN	Clock Input Reference B, Negative	Input	23	18
FBKP	Clock Feedback, Positive	Input	27	22
FBKN	Clock Feedback, Negative	Input	26	21
REFA_VTT	Termination Voltage for Reference A Input	Power	19	14
REFB_VTT	Termination Voltage for Reference B Input	Power	22	17
FBK_VTT	Termination Voltage for Feedback Input	Power	25	20
$\overline{\text{RESET}}$	Reset PLL and All Digital Circuitry	Input	55	42
USER 0	User Configurable Input / Output 0	I/O	63	48
USER 1	User Configurable Input / Output 1	I/O	62	47
USER 2	User Configurable Input 2	Input	61	46
USER 3	User Configurable Input 3	Input	60	45
VCCJ	JTAG Interface VCC	Power	50	37
TDO	JTAG TDO Output	Output	51	38
TMS	JTAG TMS Input	Input	52	39
TCK	JTAG TCK Input	Input	53	40
TDI	JTAG TDI Input	Input	54	41
GNDD	Digital GND	GND	Die Pad	Die Pad

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1µF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output driver type (LVDS, SSTL, etc.) may be selected on a bank-by-bank basis. The output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5400D family's internal analog circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5400D family's internal digital circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5400D family devices to function in JTAG chains operating at voltages differing from VCCD.

REFAP, REFAN, REFBP, REFBN – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols. Connect unused pins to ground.

REFA_VTT, REFB_VTT – These pins are used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases. Leave unused pins open.

FBKP, FBKN – This input pin provides feedback sense of the output clock signal, and can accommodate any of the single-ended logic types. Connect unused pins to ground.

FBK_VTT – This pin is used to provide a termination voltage for the feedback input when it is configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases. Leave unused pins open.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5400D device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

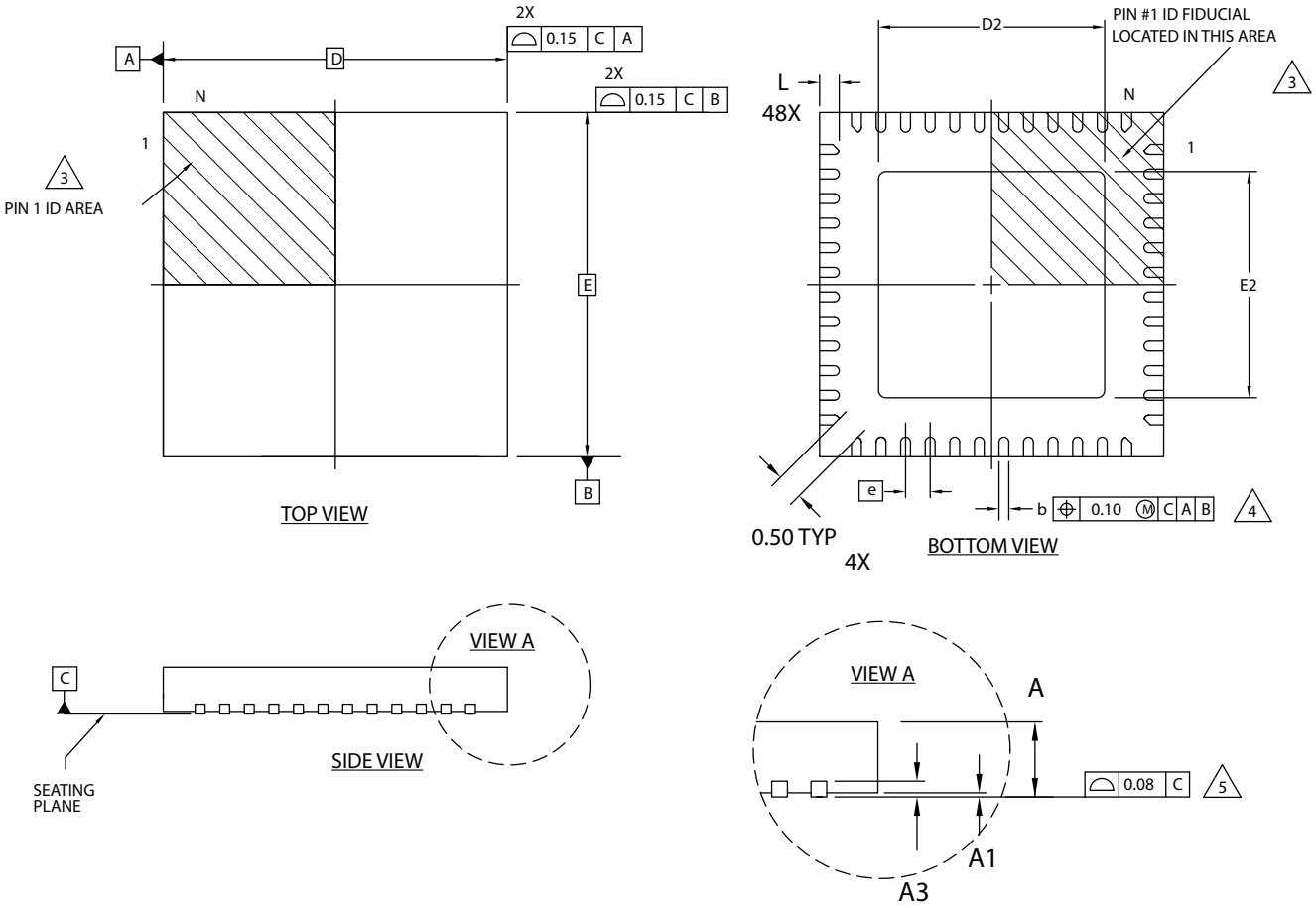
$\overline{\text{RESET}}$ – When this pin is pulled LOW, all on-board counters are reset, and lock is lost. If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

NC – These pins have no internal connection. It is recommended that they be left unconnected.

RREF – Connect a 475 Ohm (1%) between this pin and GNDD when HCSL interface is used. Leave pin open when HCSL interface is not used.

Package Diagrams

48-Pin QFNS (Dimensions in Millimeters)

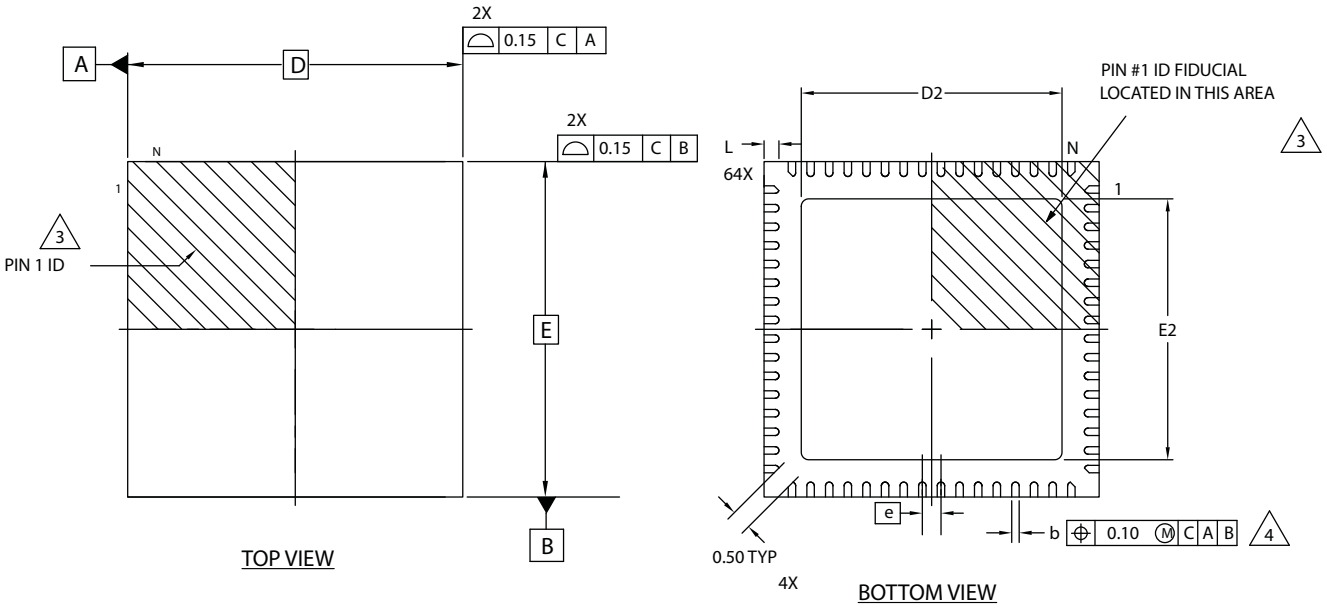


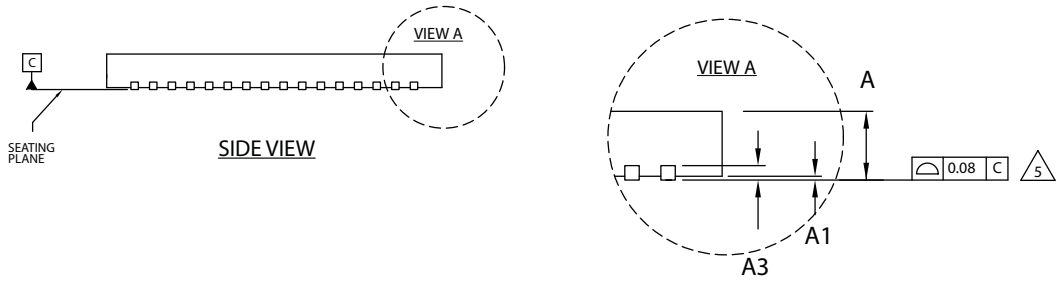
NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
5. APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		7.0 BSC	
D2	3.00	-	5.80
E		7.0 BSC	
E2	3.00	-	5.80
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

64-Pin QFNS (Dimensions in Millimeters)





NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

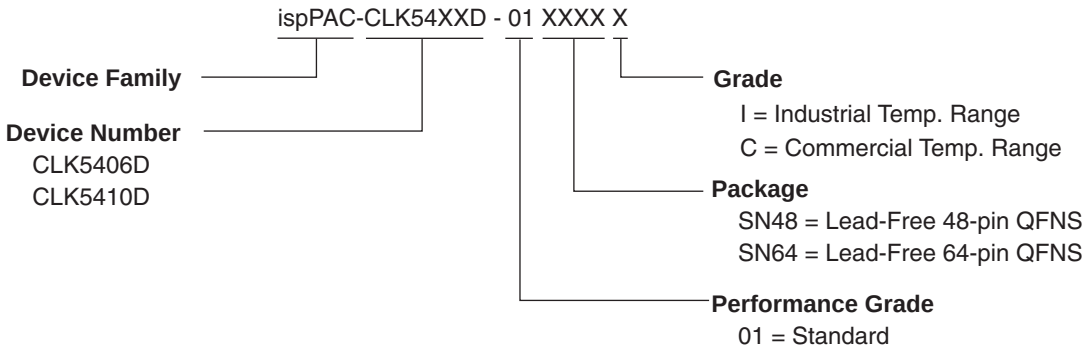
3 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

4 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.

5 APPLIES TO EXPOSED PORTION OF TERMINALS.

SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
D		9.0 BSC	
D2	5.00	-	7.50
E		9.0 BSC	
E2	5.00	-	7.50
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.30	0.40	0.50

Part Number Description



Ordering Information

Lead-Free Packaging

Commercial

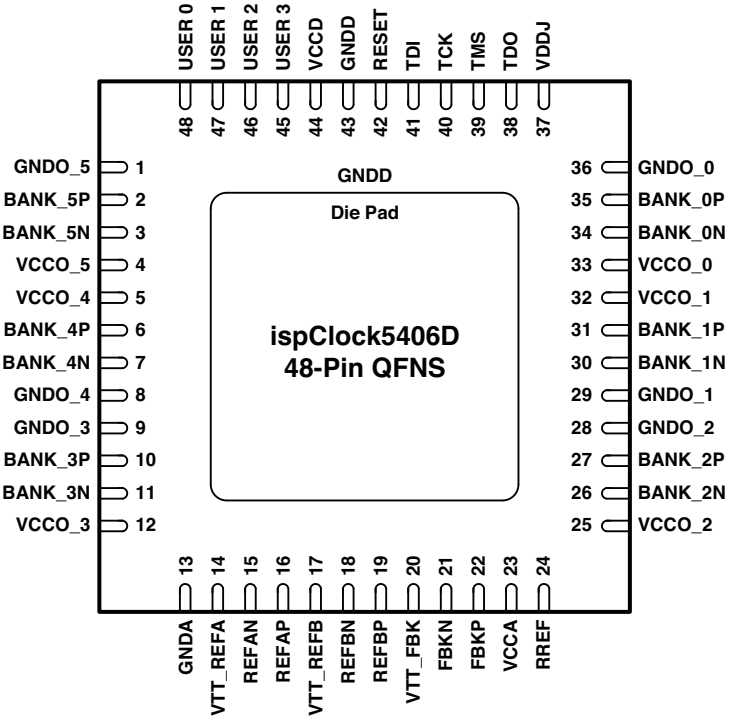
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5410D-01SN64C	10	3.3V	Lead-Free QFNS	64
ispPAC-CLK5406D-01SN48C	6	3.3V	Lead-Free QFNS	48

Industrial

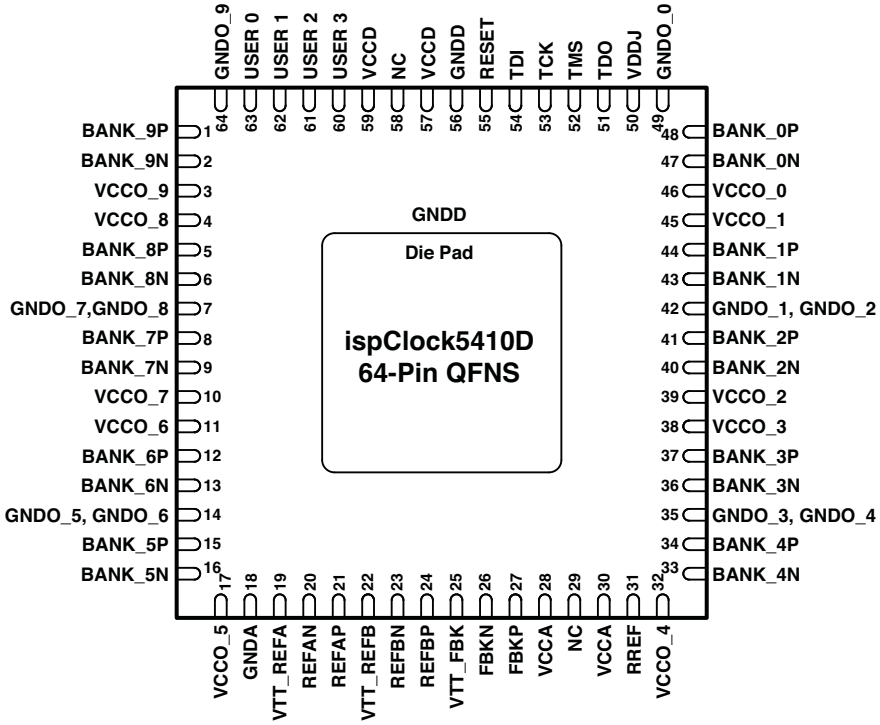
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5410D-01SN64I	10	3.3V	Lead-Free QFNS	64
ispPAC-CLK5406D-01SN48I	6	3.3V	Lead-Free QFNS	48

Package Options

ispClock5406D: 48-pin QFNS



ispClock5410D: 64-pin QFNS



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Revision History

Date	Version	Change Summary
February 2009	01.0	Initial release.
April 2009	01.1	Data sheet updated to preliminary status.
November 2009	01.2	Extended range of PLL operation.
December 2011	01.3	Corrected RREF connection for the HCSL output type.