



# MediaTek MT7681 Datasheet

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Specifications are subject to change without notice.

## Table of Contents

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<b>1</b>	<b>Introduction .....</b>	<b>4</b>
1.1	General Description .....	4
1.2	Features .....	4
1.3	Applications.....	5
1.4	Block Diagram.....	5
<b>2</b>	<b>Product Descriptions .....</b>	<b>6</b>
2.1	Pin Layout.....	6
2.2	Pin Descriptions .....	7
2.3	Strapping option.....	8
2.4	Package Information.....	9
2.5	Ordering Information .....	11
2.6	Top Marking Information.....	11
<b>3</b>	<b>Electrical And Thermal Characteristics.....</b>	<b>12</b>
3.1	Maximum And Minimum Ratings .....	12
3.2	Recommended Operating Ranges.....	12
3.3	DC Characteristics.....	13
3.4	Thermal Characteristics.....	13
3.5	Current Consumption .....	14
<b>4</b>	<b>Cautions .....</b>	<b>15</b>

## Lists of tables and figures

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Table 1 MT7681 pin descriptions.....	8
Table 2 Strapping option for the MT7681.....	8
Table 3 MT7681 ordering information.....	11
Table 4 Maximum and minimum ratings .....	12
Table 5 Recommended operating ranges.....	12
Table 6 DC characteristics.....	13
Table 7 Thermal characteristics.....	13
Table 8 WLAN 2.4GHz current consumption.....	14
Figure 1 MT7681 block diagram .....	5
Figure 2 Top view of MT7681 QFN pin-out. ....	6
Figure 3 MT7681 package outline drawing.....	9
Figure 4 MT7681 package outline drawing annotations.....	10
Figure 5 Top marking on an MT7681 chip.....	11

# 1 Introduction

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## 1.1 General Description

The MT7681 is a highly integrated Wi-Fi System on Chip (SoC), which supports IEEE802.11b/g/n single stream, GPIO and PWM for intelligent control and UART/SPI interfaces for device communication.

The MT7681 integrates a power amplifier, low noise amplifier and RF switch to reduce the module size and simplify RF design in the final product. It also integrates a power management unit for a single 3.3V power source.

A 32-bit RISC MCU is embedded in the MT7681 to run 802.11b/g/n drivers, wireless supplicant, TCP/IP protocol stack and networking applications. It also helps provide Wi-Fi station and softAP operation modes.

These features make the MT7681 a cost effective chipset for use in embedded devices that need to enable Wi-Fi-based networking services with minimal design effort.

All these features are available in a compact 40 pin, 5mm x 5mm QFN package.

## 1.2 Features

The key features of the MT7681 are:

- Single stream IEEE 802.11b/g/n
- 32-bit RISC microprocessor host MCU
- Embedded IEEE 802.11b/g/n drivers, wireless supplicant and TCP/IP stack
- Highly integrated RF PA, LNA and RF switch
- Integrated high efficiency switching regulator for single 3.3V power source
- Security support for WPA personal (WPA-PSK), WPA2 personal (WPA2-PSK) and WPA/WPA2 personal
- Operation in station or softAP modes
- Rich I/O interfaces: UART, SPI, PWM and GPIO
- All functions integrated in a compact 5mm x 5mm QFN40L package

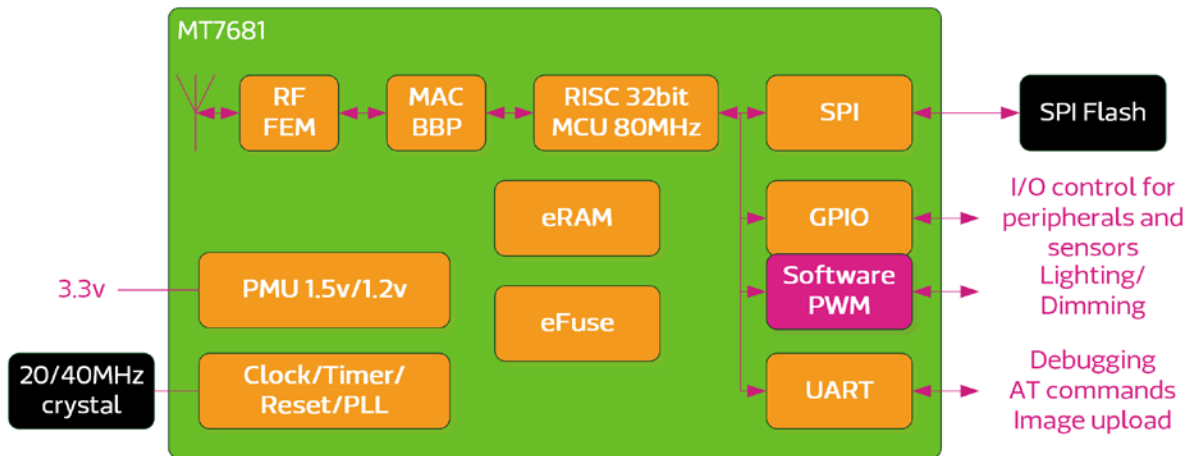
### 1.3 Applications

The MT7681 is ideal for use in devices for these applications:

- Home automation
- Smart plugs
- Lighting
- Metering
- Remote control
- Consumer network devices

### 1.4 Block Diagram

**Figure 1** shows the block diagram of the MT7681.



**Figure 1 MT7681 block diagram**

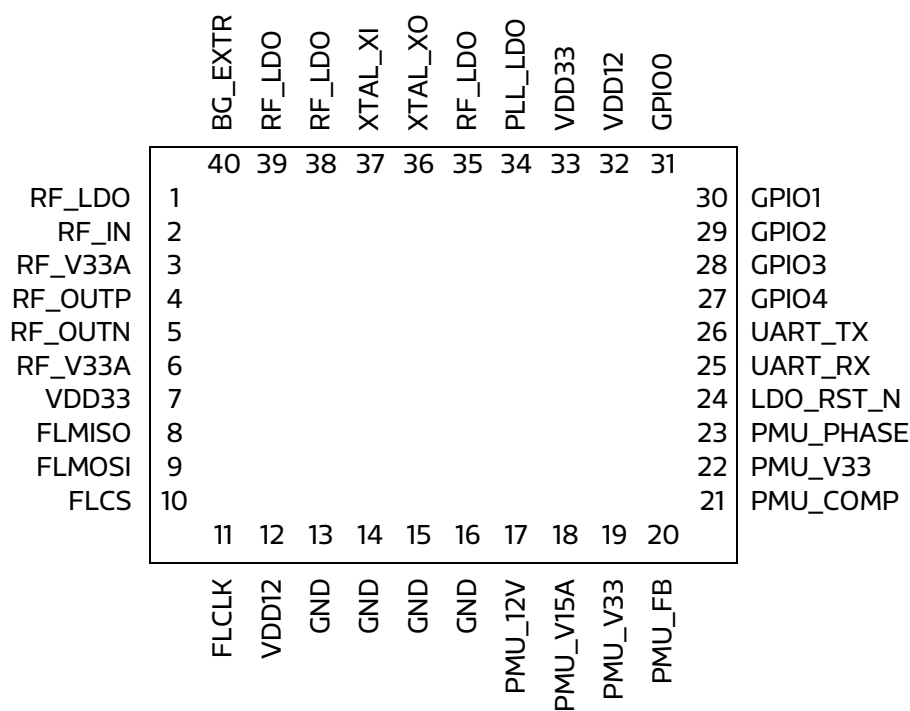
## 2 Product Descriptions

This section provides details of the MT7681, including:

- Pin layout
- Pin descriptions
- Strapping options
- Package information
- Ordering information
- Top markings

### 2.1 Pin Layout

Figure 2 shows a top view of the pin layout for the MT7681. These pins are described in detail in section 2.2, “PIN Description”.



**Figure 2 Top view of MT7681 QFN pin-out**

## 2.2 Pin Descriptions

Table 1 provides descriptions of the pins on the MT7681.

QFN40	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
<b>Reset and clocks</b>					
24	LDO_RST_N	External system reset for active low	N/A	Input	VDD33
37	XTAL_XI	Crystal or external clock input	N/A	Input	
36	XTAL_XO	Crystal output	N/A	Input	
<b>UART interface</b>					
25	UART_RX	UART Rx	N/A		VDD33
26	UART_TX	UART Tx	N/A		VDD33
<b>FLASH interface</b>					
8	FLMISO	External memory data input	PD	Input	VDD33
9	FLMOSI	External memory data output	PD	Output	VDD33
10	FLCS	External chip select	PU	Output	VDD33
11	FLCLK	External clock	PU	Output	VDD33
<b>Programmable I/O</b>					
30	GPIO0	Programmable input/output	PD	In/out	VDD33
31	GPIO1	Programmable input/output	PD	In/out	VDD33
29	GPIO2	Programmable input/output	PD	In/out	VDD33
28	GPIO3	Programmable input/output	PD	In/out	VDD33
27	GPIO4	Programmable input/output	PD	In/out	VDD33
<b>WIFI radio interface</b>					
40	BG_EXTR	RF BG reference	N/A		
2	RF_IN	RF auxiliary Rx input	N/A		
4	RF_OUTP	RF port	N/A		
5	RF_OUTN	RF port	N/A		
<b>PMU</b>					
17	PMU_12V	PMU 1.2V output	N/A	Output	
18	PMU_V15A	PMU 1.5V input	N/A	Input	
19, 22	PMU_V33	PMU 3.3V power supply	N/A	Input	
20	PMU_FB	PMU control	N/A		
21	PMU_COMP	PMU control	N/A		
23	PMU_PHASE	PMU control	N/A		
<b>Power supplies</b>					
7, 33	VDD33	Digital I/O power supply	N/A	Input	
12, 32	VDD12	Digital core power supply	N/A	Input	

QFN40	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
3, 6	RF_V33A	RF 3.3V power supply	N/A	Input	
1, 35, 38, 39	RF_LDO	RF power supply	N/A	Input	
34	PLL_LDO	PLL power supply	N/A	Input	
E-PAD	DVSS	Digital ground	N/A		

**Table 1 MT7681 pin descriptions**

## 2.3 Strapping option

Table 2 shows the strapping options for the MT7681.

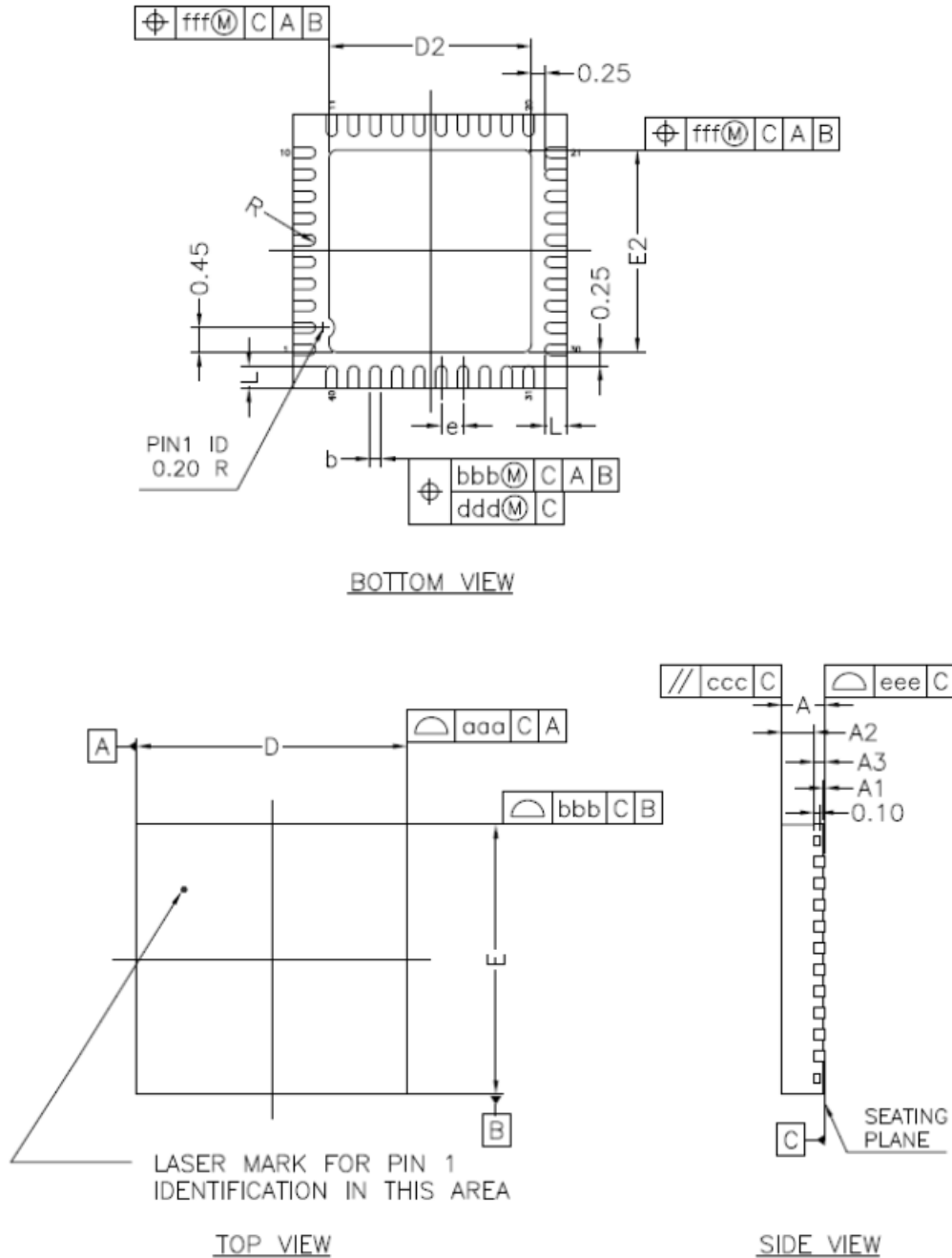
QFN40	Pin Name	Pin description	Default PU/PD
8	FLMISO	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
27	GPIO4	EXT_EE_SEL: Pull down	PD
25	UART_RX	CHIP_MODE[2]: Pull down	PD
11	FLCLK	CHIP_MODE[1]: Pull up	PD
9	FLMOSI	CHIP_MODE[0]: Pull down	PU

**Table 2 Strapping option for the MT7681**



### 2.4 Package Information

This section provides details of the QNF packaging offered on the MT7681, including the package drawings in Figure 3 and the drawing annotations in Figure 4.



**Figure 3 MT7681 package outline drawing**

\* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	----	----	0.80	----	----	0.031
A1	----	----	0.05	----	----	0.002
A2	----	0.53	0.58	----	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 bsc			0.197 bsc		
D2	3.55	3.70	3.85	0.140	0.146	0.152
E	5.00 bsc			0.197 bsc		
E2	3.55	3.70	3.85	0.140	0.146	0.152
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	----	----	0.003	----	----
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTES :

- 1.ALL DIMENSIONS ARE IN MILLIMETERS.
- 2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
- 3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
- 4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
- 5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- 6.PACKAGE WARPAGE MAX 0.08 mm.
- 7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
- 8.APPLIED ONLY TO TERMINALS.

**Figure 4 MT7681 package outline drawing annotations**

## 2.5 Ordering Information

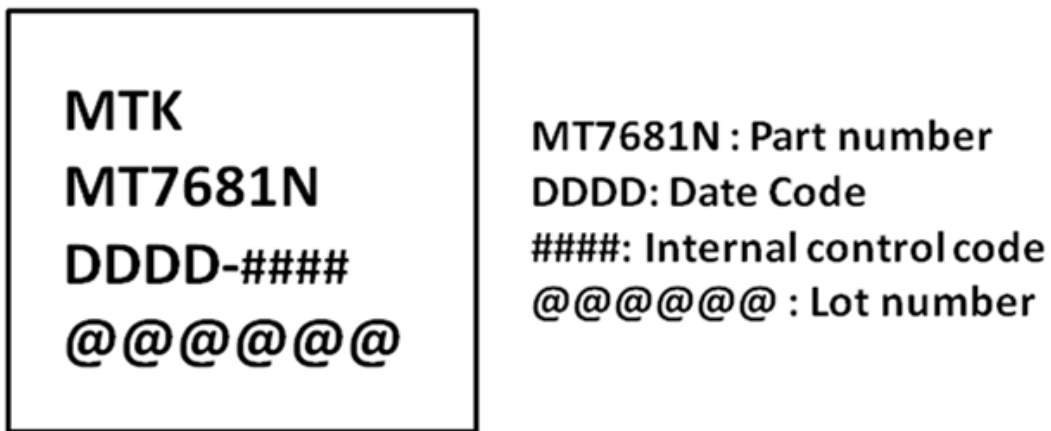
Table 3 shows the ordering information for the MT7681.

<b>Part number</b>	MT7681N
<b>Package</b>	5mm x 5mm x 0.8 mm 40-QFN
<b>Operational temperature range</b>	-10 to 70°C

**Table 3 MT7681 ordering information**

## 2.6 Top Marking Information

Figure 5 shows the top marking displayed on a MT7681 chip.



**Figure 5 Top marking on an MT7681 chip**

### 3 Electrical And Thermal Characteristics

This section provides details of the electrical and thermal characteristics of the MT7681, including:

- Maximum and minimum ratings
- Recommended operating ranges
- DC characteristics
- Thermal characteristics
- Current consumption

#### 3.1 Maximum And Minimum Ratings

Table 4 shows the maximum and minimum ratings for the MT7681.

Symbol	Parameters	Minimum rating	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3	3.6	V
VDD12	1.2V Supply Voltage	-0.3	1.5	V
VDD15	1.5V Supply Voltage	-0.3	1.8	V
T <sub>STG</sub>	Storage Temperature	-40	+125	°C
VESD	ESD protection (HBM)		2000	V

**Table 4 Maximum and minimum ratings**

#### 3.2 Recommended Operating Ranges

Table 5 shows the recommended operating ranges for the MT7681.

Symbol	Rating	Minimum	Typical	Maximum	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
T <sub>AMBIENT</sub>	Ambient Temperature	-10	-	70	°C

**Table 5 Recommended operating ranges**

### 3.3 DC Characteristics

Table 6 describes the DC characteristics of the MT7681.

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V <sub>IL</sub>	Input Low Voltage	LVTTL	-0.28	0.6	V
V <sub>IH</sub>	Input High Voltage		2.0	3.63	V
V <sub>T-</sub>	Schmitt Trigger Negative Transition Threshold Voltage	LVTTL	0.68	1.36	V
V <sub>T+</sub>	Schmitt Trigger Positive Transition Threshold Voltage		1.36	1.7	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub>   = 1.6~14 mA	-0.28	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub>   = 1.6~14 mA	2.4	VDD33+0.33	V
R <sub>PU</sub>	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R <sub>PD</sub>	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

**Table 6 DC characteristics**

### 3.4 Thermal Characteristics

Table 7 shows the thermal characteristics of the MT7681.

Symbol	Description	Performance	
		Typical	Unit
T <sub>J</sub>	Maximum Junction Temperature (Plastic Package)	125	°C
Θ <sub>JA</sub>	Junction to ambient temperature thermal resistance <sup>[1][2]</sup>	48.11	°C/W
Θ <sub>JC</sub>	Junction to case temperature thermal resistance	TBD	°C/W
Ψ <sub>Jt</sub>	Junction to the package thermal resistance <sup>[3]</sup>	3.23	°C/W

Notes:

[1] Air flow condition: Natural convection, 0.5m/s.

[2] PCB dimension 21mm x 11mm. 4-layer.

[3] 5mm x 5mm QFN40L package

**Table 7 Thermal characteristics**

### 3.5 Current Consumption

Table 8 shows the current consumption for the Wi-Fi features of the MT7681.

Description	Performance	
	Typical	Unit
Sleep mode	1.1	mA
RX Active, HT40, MCS7	151	mA
RX Power saving, DTIM=1	15	mA
RX Listen	6	mA
TX HT40, MCS7 @15dBm	210	mA
TX CCK, 11Mbps @19dBm	242	mA

Note: All results measured at the antenna port with VDD33 at 3.3V

**Table 8 WLAN 2.4GHz current consumption**

## 4 Cautions

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### **ESD CAUTION**

MT7681 is an ESD (electrostatic discharge) sensitive device and may be damaged by ESD or spike voltage. Although MT7681 has built-in ESD protection circuitry, please handle with care to avoid permanent damage or performance degradation.