PIC16C66

PIC16C66 Rev. A Silicon Errata Sheet

The PIC16C66 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30234**D**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C66 silicon.

1. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: COMPARE OUTPUT LOW SWITCHING

CCP Mode CCPxM<3:0> =	I/O pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

Work around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low, when the compare condition occurs.

2. Module: SSP Module (I^2C™ mode)

If the bus is active when the I^2C mode is enabled, and the next 8-bits of data on the bus match the address of the device, then the SSP module will generate an Acknowledge pulse.

Work around

Before enabling the I^2C mode, ensure that the bus is not active.

3. Module: Timer0

The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

Work around

Follow the following sequence:

a) Read the 8-bit TMR0 register into the W register
b) Clear the TMR0 register
c) Assign WDT postscaler to Timer0
d) Write W register to TMR0

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30234**D**), the following clarifications and corrections should be noted.

1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (parameter D150, the RA4 pin) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage. The new value is shown in Table 2.

TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D150	VOD	RA4 Open Drain High Voltage	—	—	10	—	—	14	V

2. Module: SSP (SPI Mode Timing Specifications)

The SPI interface timings (parameters 71, 71A, 72, 72A, 73, and 73A) have been modified. The new values are shown in Table 3.

TABLE 3: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
71	TSCH	SCK input high time (Slave mode)	Continuous	1.25 TCY + 30 ns	—	—	TCY + 20 ns	—	—	ns
71A			Single Byte(1)	40	—	—	N.A.			ns
72	TSCL	SCK input low time (Slave mode)	Continuous	1.25 TCY + 30 ns	—	—	TCY + 20 ns	—	—	ns
72A			Single Byte(1)	40	—	—	N.A.			ns
73A	TB2B	Last clock edge of the Byte1 to 1st clock edge of the Byte2(1)		1.5 TCY + 40 ns	—	—	N.A.			ns

* This parameter is characterized but not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

3. Module: Timer1

The operation of Timer1 needs some clarification when the timer registers are written and the TMR1ON bit is set.

The internal clock signal, that is the input to the TMR1 prescaler, affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

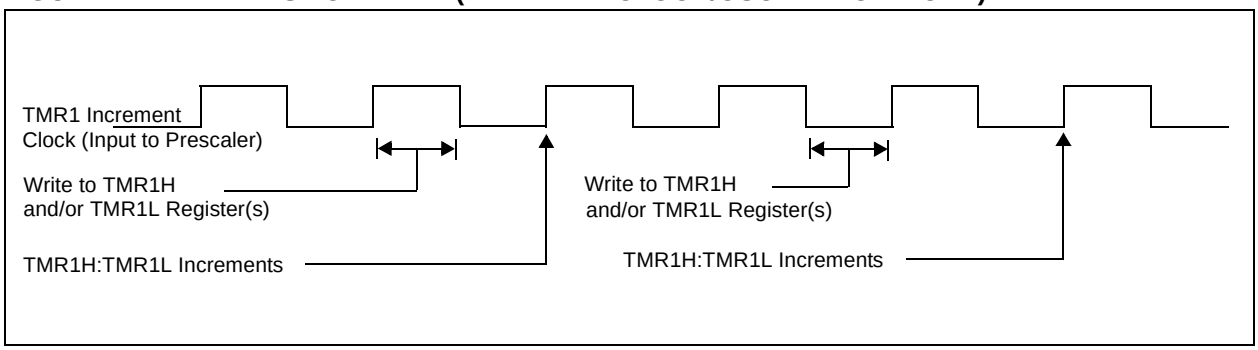
When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the V_{IH} and V_{IL} thresholds on the oscillator/clock pins, external Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK/OSCILLATOR MODE)



4. Module: RC Oscillator

The table for RC Oscillator Frequencies in the Device Characterization section of the Data Sheet is incorrect. The correct characterization information is shown in Table 4.

TABLE 4: RC OSCILLATOR FREQUENCIES CHARACTERIZATION CHANGES FROM DATA SHEET

CEXT	REXT	Correct Characterization Data		Current Data Sheet Values	
		Average	% Variation	Average	% Variation
22 pF	5.1 K	3.55 MHz	± 9.63%	4.12 MHz	± 1.4%
	10 K	1.99 MHz	± 10.53%	2.35 MHz	± 1.4%
	100 K	221.9 kHz	± 12.10%	268 kHz	± 1.1%
100 pF	3.3 K	1.77 MHz	± 10.67%	1.80 MHz	± 1.0%
	5.1 K	1.22 MHz	± 10.41%	1.27 MHz	± 1.0%
	10 K	669.4 kHz	± 10.92%	688 kHz	± 1.2%
	100 K	71.5 kHz	± 11.21%	77.2 kHz	± 1.0%
330 pF	3.3 K	625.1 kHz	± 10.68%	707 kHz	± 1.4%
	5.1 K	428.5 kHz	± 10.96%	501 kHz	± 1.2%
	10 K	231.9 kHz	± 11.32%	269 kHz	± 1.6%
	100 K	24.4 kHz	± 12.93%	28.3 kHz	± 1.1%

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from the average value for V_{DD} = 5V.

5. Module: Brown-Out Reset (BOR)

The levels specified for the BOR module thresholds (parameter D005) have changed. The new values are shown in Table 5.

TABLE 5: MINIMUM AND MAXIMUM BOR RESET VOLTAGES

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D005	V_{BOR}	Brown-out Reset Voltage	3.65	—	4.35	3.70	—	4.30	V

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Tel: 480-792-7966 Fax: 480-792-7456

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Dallas
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Addison, TX 75001
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Dayton
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Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
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Irvine, CA 92612
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Mountain View
Analog Product Sales
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Mountain View, CA 94043-1836
Tel: 650-968-9241 Fax: 650-967-1590

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai
Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong
Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

ASIA/PACIFIC (continued)

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany
Analog Product Sales
Lochhamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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