XR-T3588/89

V.35 Interface
Receiver/Transmitter

...the analog plus company™

June 1997-3

FEATURES

- Compatible with ITU-T V.35 and Bell 306 Interface Requirements
- TTL Input Compatibility
- High Common Mode Output Voltage Range
- Excellent Stability over Supply and Temperature Range
- High Speed Operation (up to 10Mbps)
- Individual Receive/Transmit Power Down Capability

APPLICATIONS

- High Speed Data Transmission Systems
- Short Haul Modems
- Signal Converters and Adapters
- Network and Diagnostic Systems
- Matrix Switches
- Modem Emulators

GENERAL DESCRIPTION

This V.35 chip set consists of two bipolar chips, one performing a receive function, the other a transmit function according to the specification requirements laid down in Appendix 11 of the V.35 ITU-T Recommendation and Bell 306 modem interface specification.

Typical applications require three transmit and receive pairs to establish the link between distant DTE's at data rates ranging from 48Kbps to 10Mbps. To conserve power (especially in the transmitter, which requires approximately 22mA or each output stage to meet ITU-T specifications), power-down functions are included in both devices, allowing any of the three receive/transmit circuits to be disabled. All inputs and outputs are TTL compatible and designed to offer maximum versatility and performance.

Both the transmitter and receiver require termination resistors external to each device, to meet the V.35 specification tolerance.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-T3588CN	18 Lead 300 Mil CDIP	0°C to 70°C
XR-T3588CP	18 Lead 300 Mil PDIP	0°C to 70°C
XR-T3589CN	14 Lead 300 Mil CDIP	0°C to 70°C

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BLOCK DIAGRAM

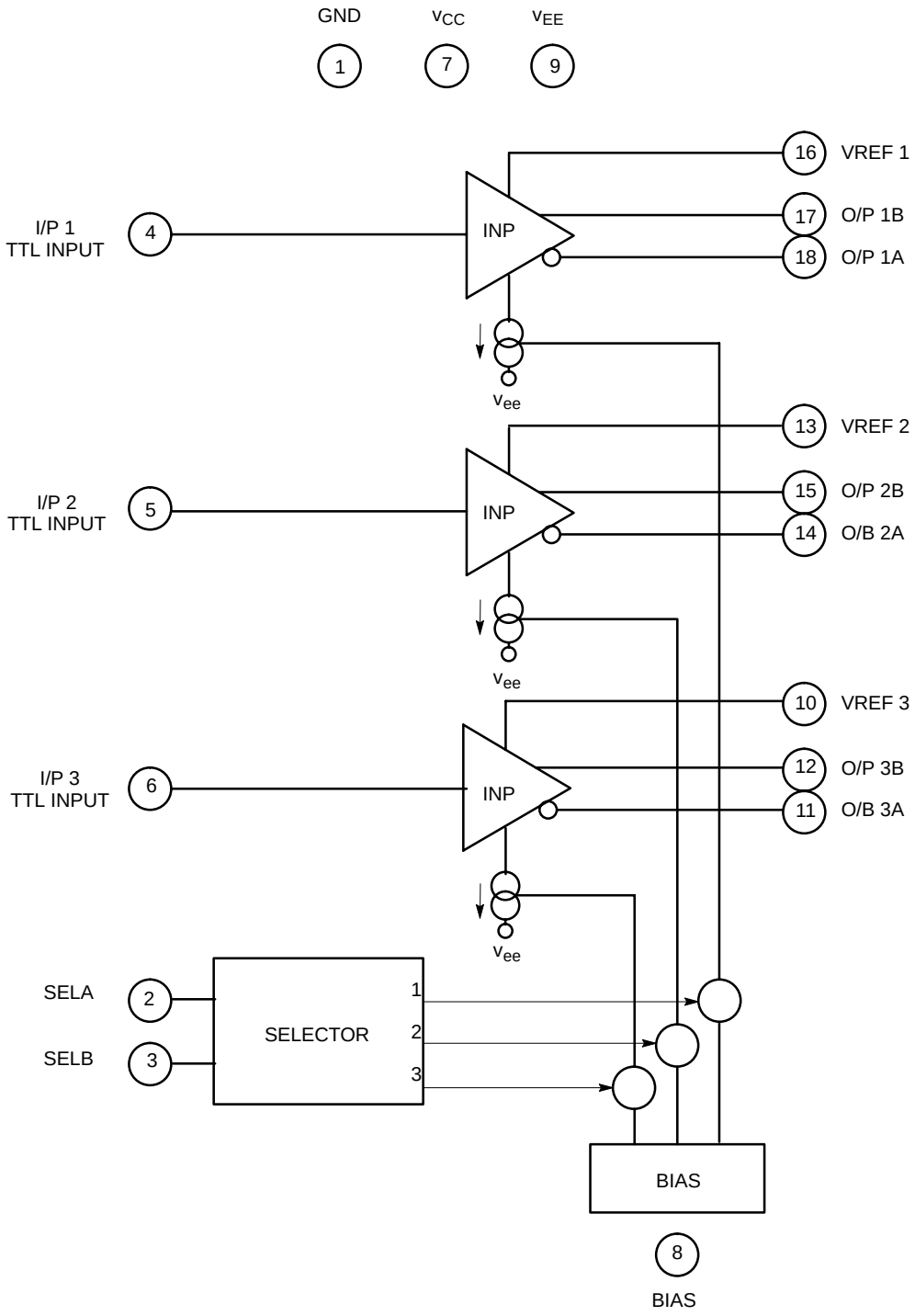


Figure 1. XR-T3588 Block Diagram

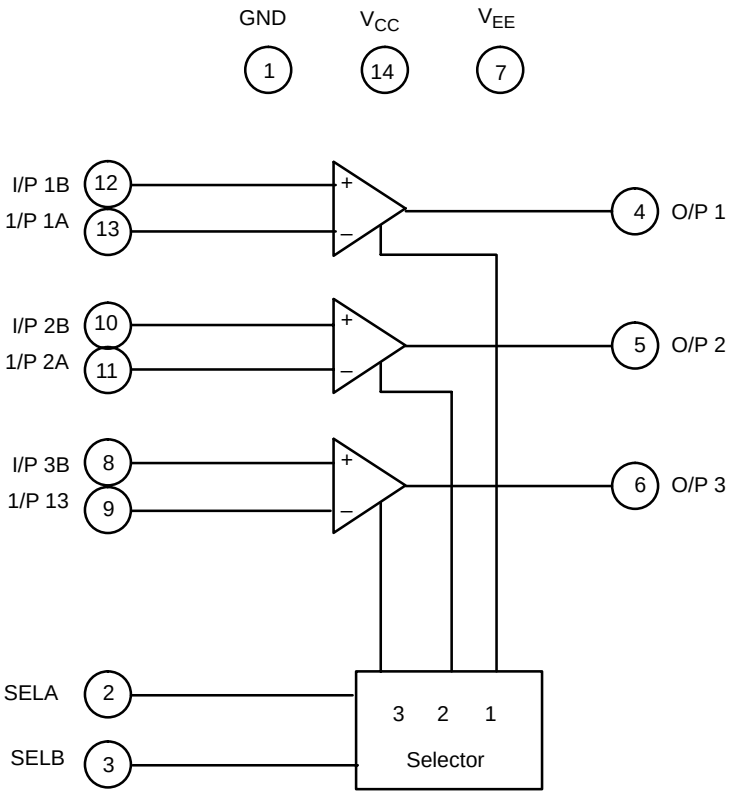
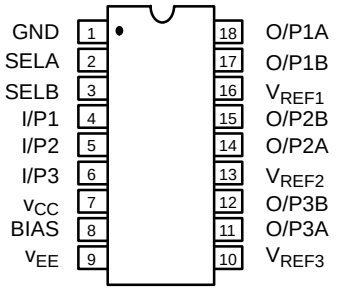
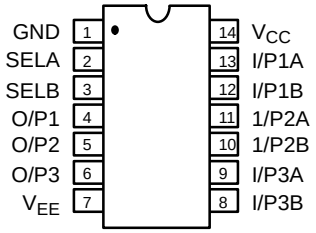


Figure 2. XR-T3588 Block Diagram

PIN CONFIGURATION



18 Lead PDIP, CDIP (0.300")
XR–T3588



14 Lead CDIP (0.300")
XR–T3589

PIN DESCRIPTION FOR XR-T3588

Pin #	Symbol	Type	Description
1	GND		**Ground (0V).**
2	SELA	I	**Channel Enable Select A Input.** TTL compatible input used in conjunction with SELB to power down individual receiver channels. (see table 2).
3	SELB	I	**Channel Enable Select B Input.** TTL compatible input used in conjunction with SELA to power down individual receiver channels (see table 2).
4	I/P1	I	**Channel 1 Input.** TTL compatible.
5	I/P2	I	**Channel 2 Input.** TTL compatible.
6	I/P3	I	**Channel 3 Input.** TTL compatible.
7	V_{CC}		**Positive Supply (5V).**
8	BIAS	I	**Bias Current Input.** DC level 1.1V nominal. Connect external resistor from pin to ground to define transmitter output current levels (R_{bias} 3.9k for Iout=22mA).
9	V_{EE}		**Negative Supply (-5V).**
10	V_{REF3}	O	**Channel 3 Voltage Regulator**. Provides 3.3V regulated supply for connection of channel 3 transmit termination network (see *Figure 6*). If the driver is disabled, the voltage output at this pin will be Vcc - 0.7V.
11	O/P3A	O	**Channel 3 Differential Output A.** Open collector current output. Current sink capability 22mA nominal (defined by Rbias). When terminated with network to VREF3 provides an output voltage with inverse phase to I/P3. DC level with TX and RX termination +/-O.275V nominal.
12	O/P3B	O	**Channel 3 Differential Output B**. Open collector current output. Current sink capability 22mA nominal (defined by Rbias). When terminated with network to VREF3 provides an output voltage in phase with I/P3. DC level with TX and RX termination +/-O.275V nominal.
13	V_{REF2}	O	**Channel 2 Voltage Regulator.** Provides 3.3V regulated supply for connection of channel 2 transmit termination network (see *Figure 6*). If the driver is disabled, the voltage output at this pin will be Vcc - 0.7V.
14	O/P2A	O	**Channel 2 Differential Output A.** Open collector current output. Current sink capability 22mA Nominal (Defined by Rbias). When terminated with network to VREF2 provides an output voltage with inverse phase to I/P2. DC level with TX and RX termination +/-o.275V nominal.
15	O/P2B	O	**Channel 2 Differential Output B.** Open collector current output. Current sink capability 22mA nominal (defined by Rbias). When terminated with network to VREF2 provides an output voltage in phase with I/P2. DC level with TX and RX termination +/-O.275V nominal.

PIN DESCRIPTION FOR XR-T3588 (CONT'D)

Pin #	Symbol	Type	Description
16	V_{REF1}	O	**Channel 1 Voltage Regulator.** Provides 3.3V regulated supply for connection of channel 1 transmit termination network (see *Figure 6*). If the driver is disabled, the voltage output at this pin will be Vcc - 0.7V.
17	O/Pl B	O	**Channel l Differential Output B.** Open collector current output. Current sink capability 22mA nominal (defined by Rbias). When terminated with network to VREF1 provides an output voltage in phase with I/P2. DC level with TX and RX termination +/-O.275V nominal.
18	O/Pl A	O	**Channel 1 Differential Output A.** Open collector current output. Current sink capability 22mA nominal (defined by Rbias). When terminated with network to VREF2 provides an output voltage with inverse phase to I/Pl. DC level with TX and RX termination +/-O.275V nominal.

PIN DESCRIPTION FOR XR-T3589

Pin #	Symbol	Type	Description
1	GND		**Ground (0V).**
2	SELA	I	**Channel Enable Select A Input.** TTL compatible input used in conjunction with SELB to power down individual receiver channels. (see table 2).
3	SELB	I	**Channel Enable Select B Input.** TTL compatible input used in conjunction with SELA to power down individual receiver channels (see table 2).
4	O/P1	O	**Channel 1 Output.** TTL compatible.
5	O/P2	O	**Channel 2 Output.** TTL compatible.
6	O/P3	O	**Channel 3 Output.** TTL compatible.
7	V_{EE}		**Negative Supply (-5V).**
8	I/P3B	I	**Channel 3 Differential Input B.** Rin 4kL2 nominal. Should be terminated with an external network to GND (see *Figure 8*).
9	I/P3A	I	**Channel 3 Differential Input A.** Rin 4k.Q nominal. Should be terminated with an external network to GND (see *Figure 8*).
10	VP2B	I	**Channel 2 Differential Input B.** Rin 4kL2 nominal. Should be terminated with an external network to GND (see *Figure 8*).
11	I/P2A	I	**Channel 2 Differential Input A.** Rin 4kQ nominal. Should be terminated with an external network to GND (see *Figure 8*).
12	I/Pl B	I	**Channel l Differential Input B.** Rin 4k.Q nominal. Should be terminated with an external network to GND (see *Figure 8*).
13	I/PlA	I	**Channel l Differential Input A.** Rin 4k.Q nominal. Should be terminated with an external network to GND (see *Figure 8*).
14	V_{CC}		**Positive Supply (5V).**

XR-T3588 ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Electrical Characteristics						
V_{CC}	Positive Supply Voltage	4.75	5	5.25	V	
V_{EE}	Negative Supply Voltage	-4.75	-5	-5.25	V	
I_{CC}	Input Current		86	124	mA	[1]
I_{EE}	Input Current	-132	-92		mA	[1]
I_{PCC}	Power Down I_{CC}	0.2		10.2	mA	[2]
I_{PEE}	Power Down I_{EE}	-1.0		-14.0	mA	[2]
V_{DIH}	High Level Input Voltage	2		V_{CC}	V	Data Inputs
I_{DIL}	Low Level Input Voltage	0		0.8	V	Data Inputs
I_{DIH}	Input Current High			1.0	µA	Data Inputs
I_{DIL}	Input Current Low	-2.1			mA	Data Inputs
V_{SIH}	Selector High Level Voltage	2		V_{CC}	V	
V_{SIL}	Selector Low Level Voltage	0		0.6	V	
I_{SIL}	Selector Input Current Low	-0.6			mA	
I_{SIH}	Selector Input Current High			50	µA	
V_{OL}	Output Low Voltage	-0.91			V	[3]
V_{OH}	Output High Voltage			0.85	V	[3]
ZS	Source Impedance	90	100	110	Ω	Per CCITT V.35[4,5,6]
RGND	Resistance to Ground	135	150	165	Ω	Per CCITT V.35[4,5,6]
IODIFF	Output Current Differential	20.2	22.0	23.8	mA	With 3.9K Bias Resistor
V_{REF}	Transmitter Reference Voltage	3.0	3.3	3.6	V	Voltage Output
AC Electrical Characteristics[6] (see *Figure 3*)						
t_{PLHT}	Input to Output		25	50	ns	
t_{PHLT}	Input to Output		25	50	ns	
t_{RT}	TX Rise Time		10	20	ns	
t_{FT}	TX Fall Time		10	20	ns	

Notes

[1] With extemal transmit network (Figure 6) connected to each transmitter output and select A, select B both high.

[2] All transmitter outputs open-circuit and select A, select B both low.

[3] With extemal transmit network terminated with 100Ω (Figure 7).

[4] Differential impedance between O/P A and O/P B. extemal transmit network (Figure 6) connected to transmitter output.

[5] O/P A's and O/P Bs connected together, resistance measured to ground, extemal transmit network ((Figure 6) present.

[6] O/P terminated with extemal transmit network terminated with 100Ω (See Figure 7).

Specifications are subject to change without notice

XR-T3589 ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±5%, V_{EE} = -5V ±5%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Electrical Characteristics						
Vcc	Supply Voltage	4.75	5	5.25	V	
V_{EE}	Supply Voltage	-5.25	-5	-4.75	V	
I_{CC}	Input Current		40	60	mA	Select A, Select B, Both High
I_{EE}	Input Current		7	9	mA	Select A, Select B, Both High
I_{OH}	Output High Level Current	-1.6			µA	$V_{OH} \geq 2.4V$
I_{OL}	Output Low Level Current			40	mA	$V_{OL} < 0.4V$
V_{OH}	High Level Output	2.4			V	at $I_{OH} < 40\mu A$
V_{OL}	Low Level Output			0.4	V	at $I_{OL} < 1.6mA$
V_{IN}	Input Sensitivity	400			mV	Differential[2]
Z_{INO}	Input Impedance	8			kΩ	$Differential_2$
Z_{INT}	Input Impedance	90	100	110	Ω	Per ITU-T V.35[1, 2]
R_{GND}	Resistance to GND	135	150	165	Ω	Per ITU-T V.35[1, 2]
V_{SIH}	Select High Level Voltage	2		V_{CC}	V	
V_{SIL}	Select Low Level Voltage			0.8	V	
I_{PCC}	Power Down I_{CC} Current		1.1		mA	Select A, Select B, Both Low
I_{PEE}	Power Down I_{EE} Current	-0.3			mA	
AC Electrical Characteristics (see *Figure 4*)						
t_{PLHR}	Input to Output		50	70	ns	
t_{PHLR}	Input to Output		50	70	ns	
t_{RR}	RX Rise Time		18	40	ns	
t_{FR}	RX Fall Time		12	30	ns	

Notes

[1] I/P terminated to circuit 102 (see Figure 8.)

[2] Pins 8-9, 10-11, 12-13.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Voltages . . . . . ±7V

Storage Temperature . . . . . -65°C to + 150°C

Power Dissipation . . . . . .

XR-T3588CN 1000mW

XR-T3589CN 300mW

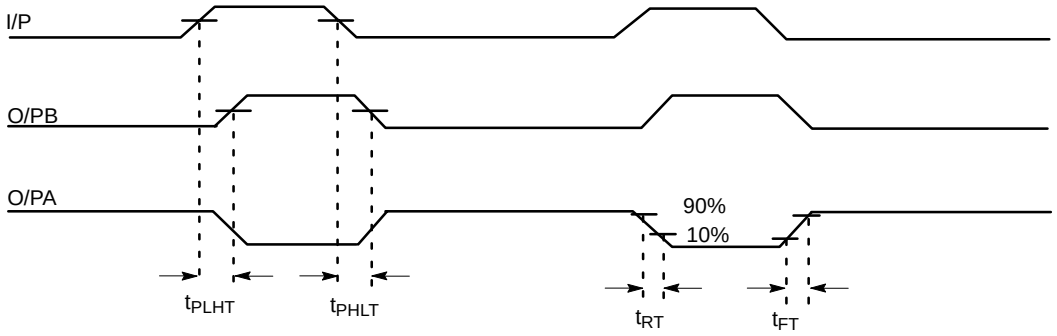


Figure 3. Transmitter Waveforms

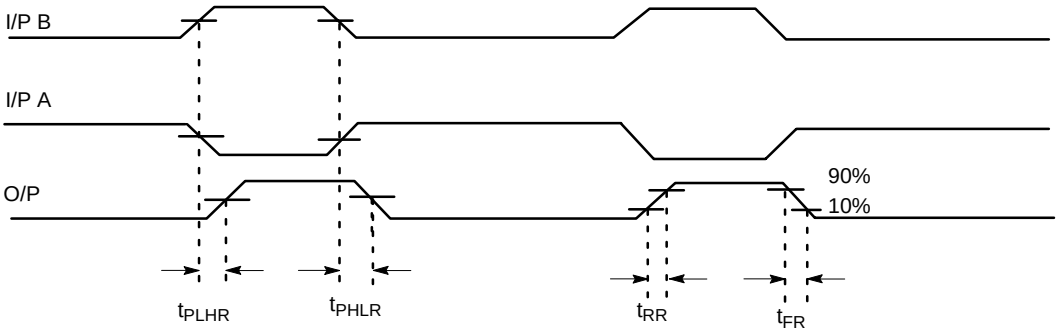


Figure 4. Receiver Waveforms

SYSTEM DESCRIPTION

XR–T3588

The function of the transmitter is to take a TTL input signal at a maximum bit rate of 1OMbps and output a balanced differential signal with a peak amplitude of 0.55V and a maximum DC offset of 0.6V. An internal buffer provides the regulated output voltage to set the mean level of the transmitters to less than 0.6V. *Figure 5* shows a simplified circuit for the output stage.

To meet the pulse shape and offset requirements laid down in the V.35 specification, the transmitter employs an internal temperature compensated voltage generator to provide reference voltages for both offset control and output current generation. Load resistors for the output stage, which provide the required source impedance for the transmitter, are external to the IC and are required to meet the V.35 specified tolerance.

XR–T3589

The XR-T3589 Line Receiver contains three identical receive circuits to complement the XR-T3588 Line Transmitter. Received differential signals are converted into a single TTL compatible output. The input stage is designed to meet the full V.35 noise and common mode input specification.

Individual receivers may be shut down to achieve power savings for applications not requiring three channels. Two TTL compatible inputs provide four combinations of transmitter configurations, as defined in table 2. If either of the select pins is left open a high state is adopted, hence with no inputs applied, all channels are powered up. However it is recommended to tie all select inputs to either GND or V_{CC}.

Transmitter		SEL A	SEL B
1-2-3	ON	HIGH	HIGH
1-2	ON	HIGH	LOW
1	ON	LOW	HIGH
ALL	OFF	LOW	LOW

Table 1. Transmitter Selectors

Transmitter		SEL A	SEL B
1-2-3	ON	HIGH	HIGH
1-2	ON	HIGH	LOW
1	ON	LOW	HIGH
ALL	OFF	LOW	LOW

Table 2. Receiver Selectors

TYPICAL APPLICATIONS

Figure 9 shows a schematic for a typical application of the XR-T3588/T3589. In this application the termination resistor network is fed from the chip on-board regulator. The regulator provides a voltage of 3.3V.

The major issue is the power dissipation of the XR-T3588. Following is a discussion of the power that is dissipated by the XR-T3588 when all three drivers are active simultaneously. The power used by the XR-T3588 is given by;

$Pd = (V_{CC} - I_{CC} + V_{EE} - I_{EE}) - 3 - (Rterm - (Iterm)^2)$

Where: V_{CC}, I_{CC}, V_{EE} and I_{EE} are the positive and negative supply voltages and currents, whose values may be found in the typical column of the DC Characteristics,

Rterm is the equivalent impedance of the termination network,

Iterm is the current flow through the termination network.

In the case of the three drivers enabled and terminated, the typical power dissipation is;

$Pd = (5 - 0.086 + (5 - 0.092)) - 3 - (150 - (0.022)^2)$
$= 672.2mW$

The junction temperature of the part is given by;

$Tjunction = Tambient + (\theta_{JA} - Pd)$

where: $T_{junction}$ is junction temperature,
Tambient is ambient temperature,
θJA is package thermal impedance.

For reliable operation, the absolute maximum junction temperature must be maintained below 150°C. With a θJA for the ceramic package of 80°C/W, and a maximum ambient temperature of 70°C the junction temperature is;

Tjunction = 70 + 80 - 0.672 = 1 34°C

If the device is used in an enclosure without forced cooling where the ambient temperature could approach or exceed 70°C, the power dissipation of the part should be reduced for improved reliability.

Figure 10 shows an implementation using an external reference voltage made with two resistors of values 180Ω and 360Ω. This implementation offers the advantage of eliminating the feeding current to the termination network from the on chip reference, thereby reducing the dissipation in the XR-T3588.

The formula to calculate the on chip power dissipation is now;

$Pd = (V_{CC} - I_{GG} + V_{EE} - I_{EE}) - 3 - ((V_{CC} - 3.3) - I_{term} + R_{term} - (i_{term})^2)$

Where the term "3 - (V_{CC} - 3.3) - (Iterm)" is the power previously dissipated in the XR-T3588 internal voltage regulator.

The revised value of power dissipation is;

$Pd = (5 - 0.086) + (5 - 0.092) - 3 - ((5 - 3.3) - 0.022 + 150 - (0.022)^2) = 560mW$

The total on chip power saving is;
3 - (5 - 3.3) - 0.022, i.e. 112.2 mW.

Figure 11 shows the demo board schematic.

To obtain a demo board, call your local representative.

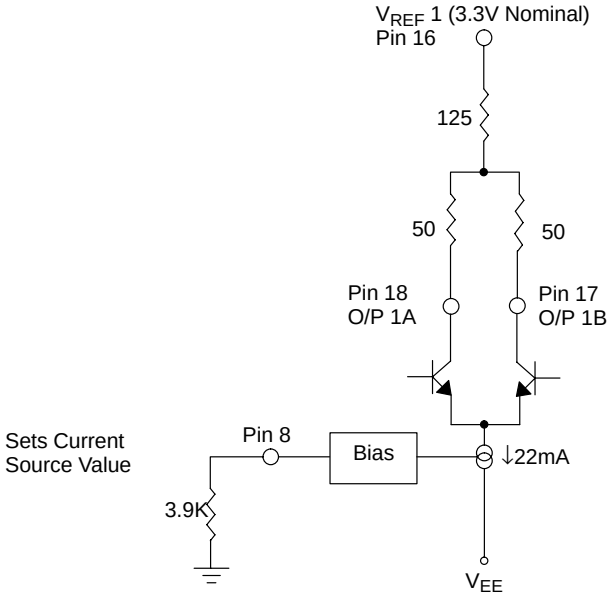


Figure 5. XR-T3588 Output Stage Simplified Circuit

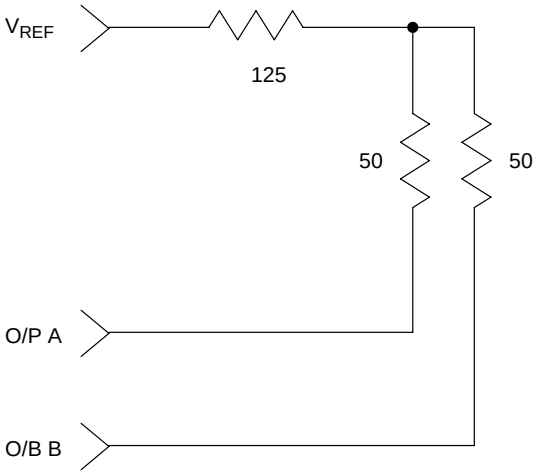


Figure 6. External Transmit Network

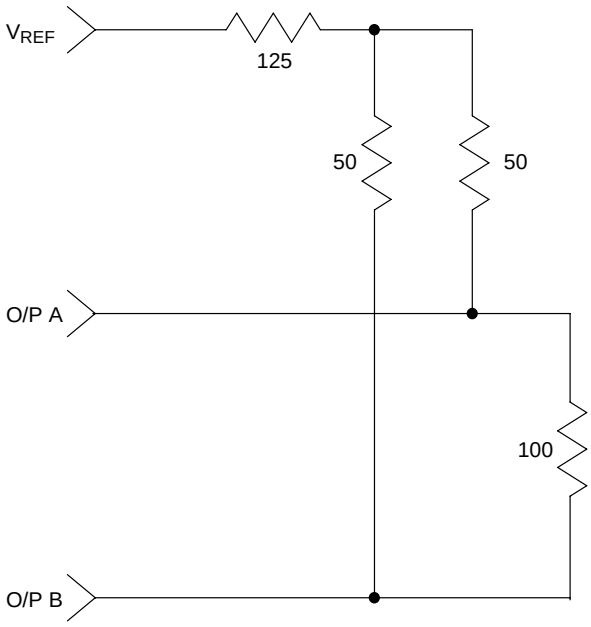


Figure 7. XR-T3588 Output Stage Simplified Circuit

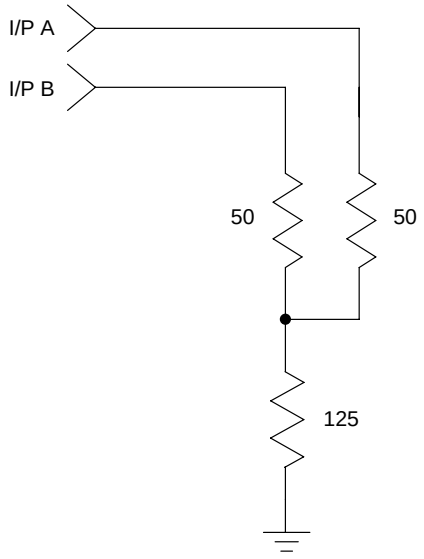
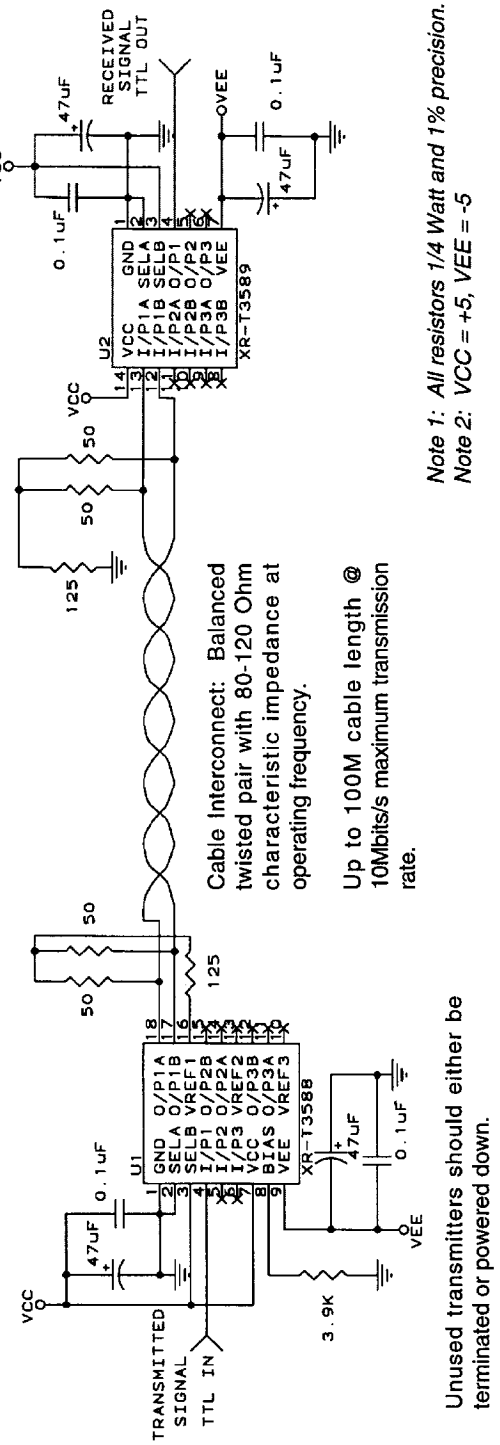


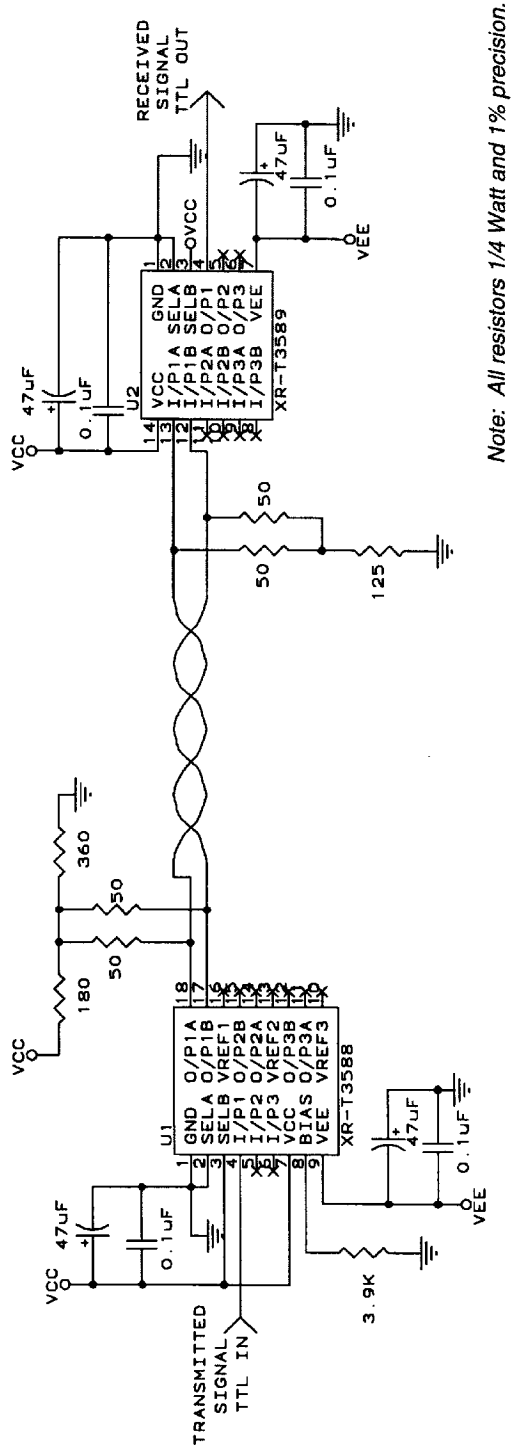
Figure 8. External Receive Network



Unused transmitters should either be terminated or powered down.

Note 1: All resistors 1/4 Watt and 1% precision.
Note 2: VCC = +5, VEE = -5

Figure 9. Application Circuit XR-T3588, XR-T3589



Note: All resistors 1/4 Watt and 1% precision.

Figure 10. Typical Low Power Dissipation

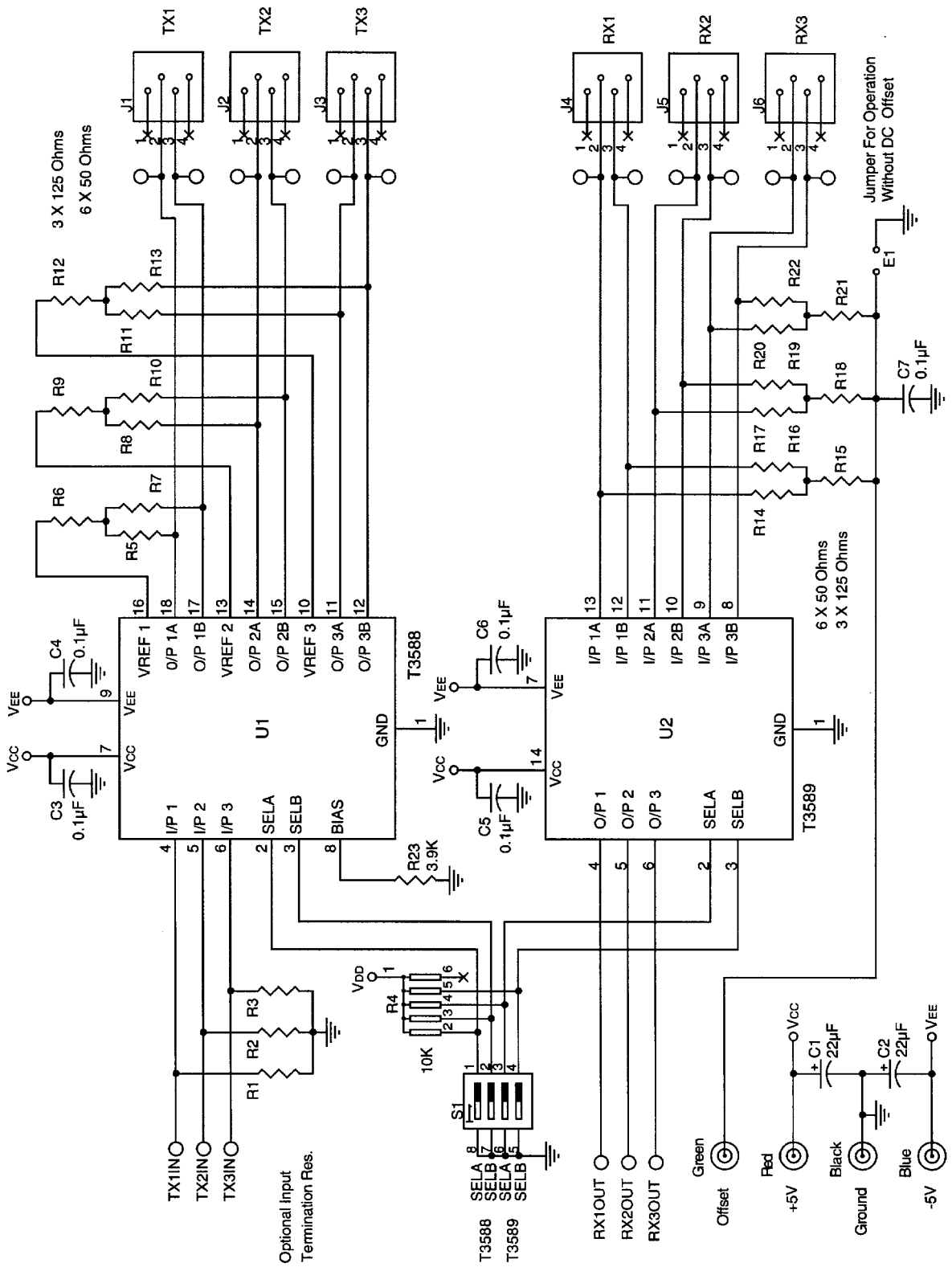
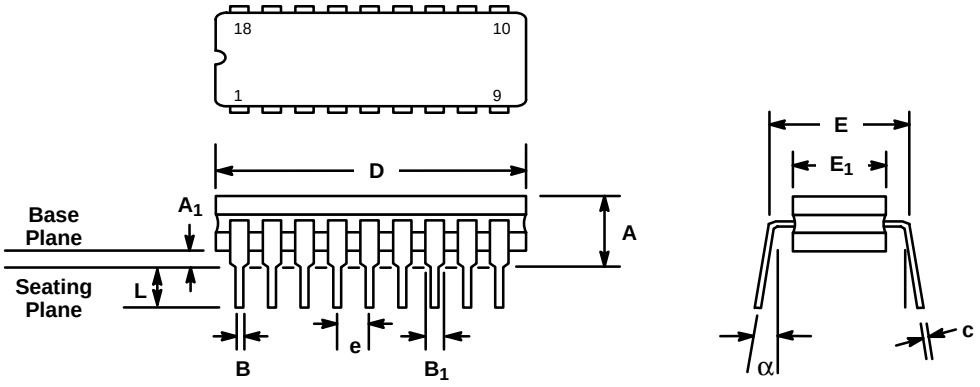


Figure 11. Demo Board Schematic

18 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

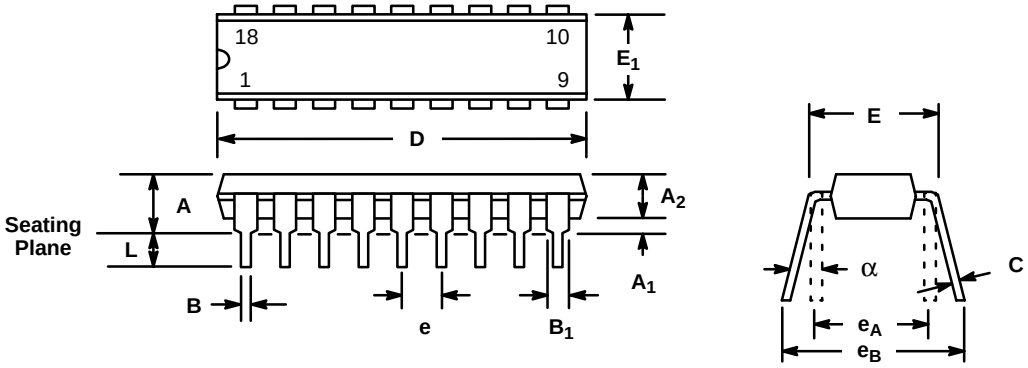


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.070	0.38	1.78
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.860	0.960	21.84	24.38
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

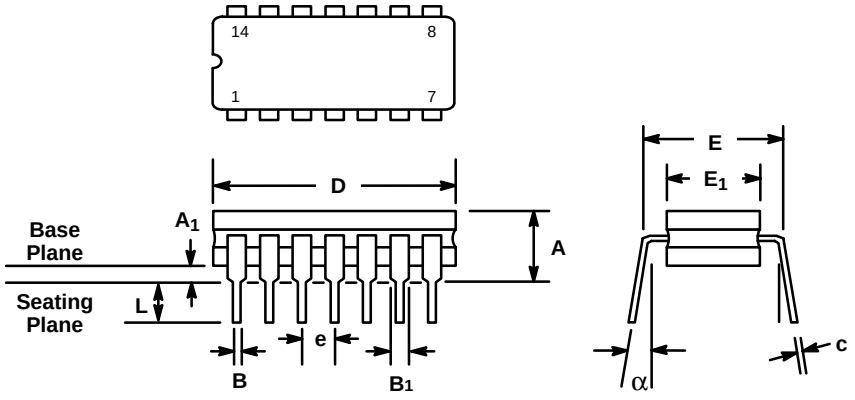


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.845	0.925	21.46	23.50
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

NOTICE

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Datasheet June 1997