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LV5685PV

Bi-CMOS LSI

System Power Supply IC for Automotive Infotainment Multiple-Output Linear Voltage Regulator

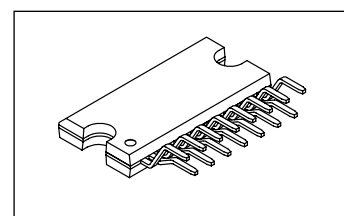
Overview

The LV5685PV is a multiple output linear regulator IC, which allows reduction of quiescent current. The LV5685PV is specifically designed to address automotive infotainment systems power supply requirements.

The LV5685PV integrates 5 linear regulator outputs, 2 high side power switches, I²C-bus communication, ACC detection, battery voltage detection, over-current limiter, overvoltage protection and thermal shut down. Supply for V_{DD} and SW33V outputs is low voltage specification, which enables drastic reduction of power dissipation compared to the existing model.

Function

- Low consumption current: 65μA (typ, only V_{DD} output is in operation)
- 5 regulator outputs
 - V_{DD} for microcontroller: output voltage: 3.3V, maximum output current: 350mA
 - For system: output voltage: 3.3/5V(set by I²C-bus), maximum output current: 450mA
 - For audio: output voltage: 5/8.5/9/11.5V(set by I²C-bus), maximum output current: 250mA
 - For illumination: output voltage: 5/8/10.5/12V(set by I²C-bus), maximum output current: 300mA
 - For CD: output voltage: 5/6/7/8V(set by I²C-bus), maximum output current: 1300mA
- 2 high side switches
 - EXT: Maximum output current: 350mA, voltage difference between input and output: 0.5V
 - ANT: Maximum output current: 300mA, voltage difference between input and output: 0.5V
- ACC detection circuit
 - detection voltage 2.7/3.2/3.6/4.2V (set by I²C-bus)
- Battery voltage detection (BDET) : V_{CC2}
 - Low voltage detection(UVDET): detection voltage 6/7/7.8/9V(set by I²C-bus)
 - Over voltage detection(OVDET): detection voltage 18V
- FLG output
 - CMOS output of ACC-detection/UVDET/OVDET/OVP
- I²C-bus communication interface
 - Each output except V_{DD} is independently enabled/disabled. ILM/CD/AUDIO/ACC/UV voltage setting.
 - Read back supported: Output voltage setting, Output over-current, FLG(ACC/UV/OVDET/OVP)
- Supply input
 - V_{6IN}: 6V for V_{DD}, system(SW33V)
 - V_{CC1}: For internal reference voltage, control circuitry
 - In case of voltage drop of V_{6IN}, V_{CC1} supplies V_{DD} output.
 - V_{CC2}: For AUDIO/ILM/CD/EXT/ANT
- Over-current protection
- Overvoltage protection(OVP):
 - V_{CC1}, V_{CC2} Typ 23V (All outputs except V_{DD} are turned off)
- Thermal shutdown: Typ 175°C



HZIP15

* I²C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

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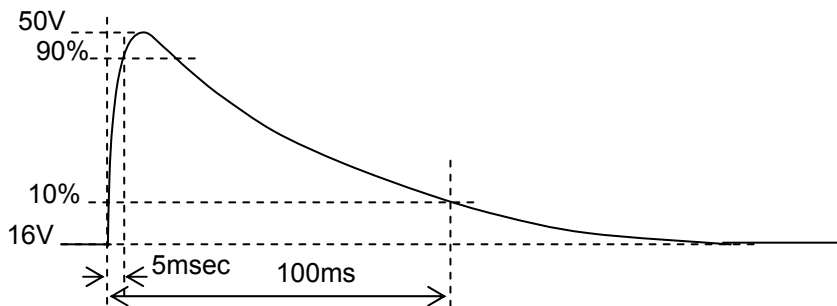
Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

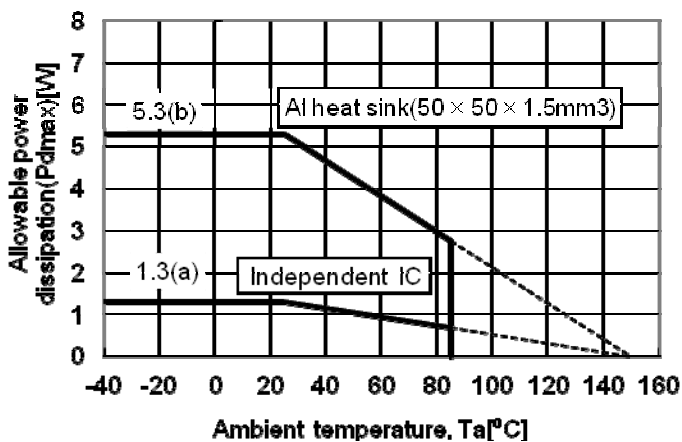
| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|---------------------------------------|---|-------------|------------------|
| Supply voltage | Vcc max | VCC1,VCC2 | 36 | V |
| | V6in max | V6IN | 7 | |
| Input voltage | Vio max | SDA,SCL,FLG | 7 | V |
| | | ACCIN | 36 | |
| Allowable power dissipation | Pd max $T_a \leq 25^\circ\text{C}$ | -Independent IC | 1.3 | W |
| | | -Al heatsink ($50 * 50 * 1.5\text{mm}^3$) is used | 5.3 | |
| | | -Size of heatsink: infinite | 26 | |
| Peak supply voltage | Vcc peak | VCC1/VCC2/ACCIN • See the test waveform below | 50 | V |
| Operating ambient temperature | Topr | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | Tstg | | -55 to +150 | $^\circ\text{C}$ |
| Junction temperature | Tjmax | | +150 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Waveform of surge test (VCC1,VCC2,ACCIN)



- Allowable power dissipation derating curve



(a) Independent IC
 (b) Aluminum heat-sink ($50 \times 50 \times 1.5\text{mm}^3$)
 Heat-sink tightening condition
 tightening torque: $39\text{N}\cdot\text{cm}$,
 with silicone grease

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Recommended Operating Conditions at Ta = 25°C

■VCC1

| Parameter | Conditions | Ratings | Unit |
|---------------------------|------------|---------|------|
| Operating supply voltage1 | VDD output | 7 to 16 | V |

■VCC2

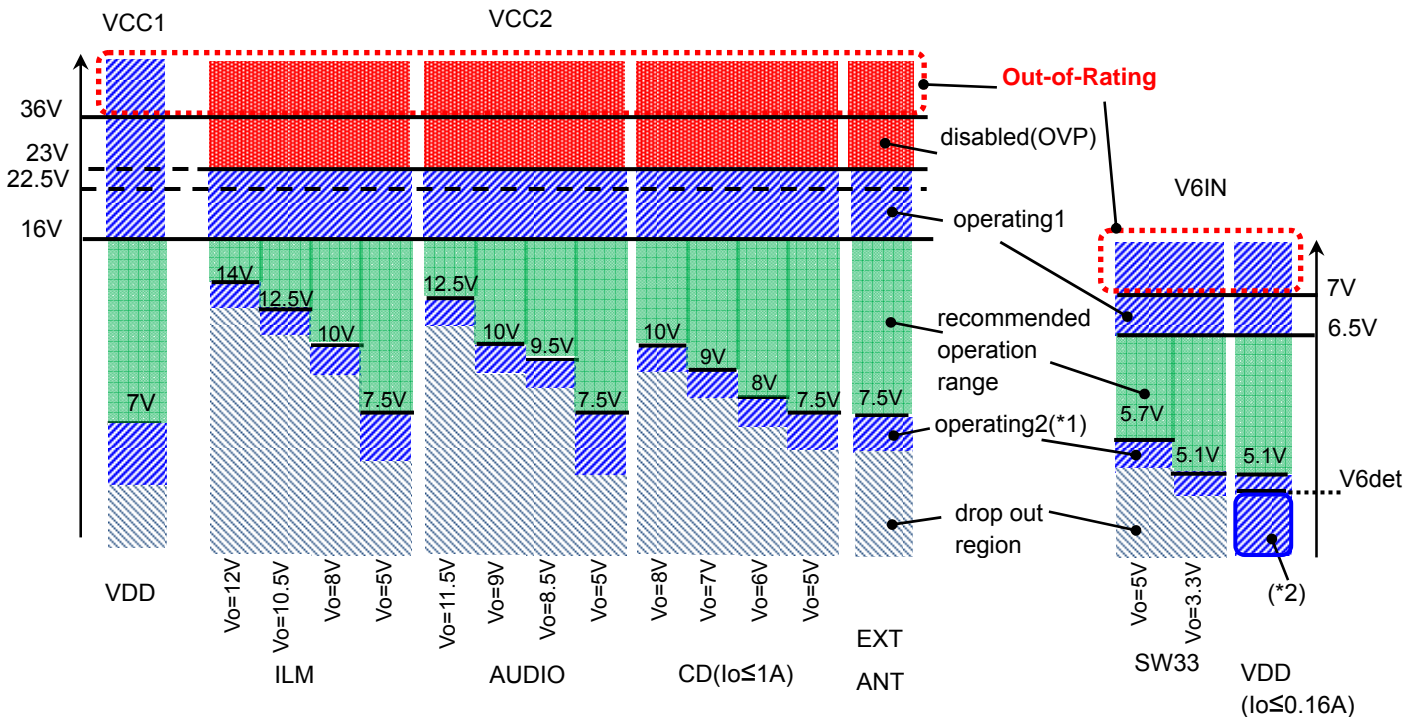
| Parameter | Conditions | Ratings | Unit |
|---------------------------|------------------------|------------|------|
| Operating supply voltage2 | ILM(10.5V) output | 12.5 to 16 | V |
| | ILM(8V) output | 10 to 16 | |
| Operating supply voltage3 | AUDIO(8.5V) output | 9.5 to 16 | V |
| Operating supply voltage4 | CD(8V) output(Io=1.3A) | 10.5 to 16 | V |
| | CD(8V) output(Io≤ 1A) | 10 to 16 | |
| Operating supply voltage5 | EXT output, ANT output | 7.5 to 16 | V |

■V6IN

| Parameter | Conditions | Ratings | Unit |
|---------------------------|--------------------|------------|------|
| Operating supply voltage6 | VDD output | 5.1 to 6.5 | V |
| | SW33V(3.3V) output | 5.1 to 6.5 | V |
| | SW33V(5V) output | 5.7 to 6.5 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

• "Maximum Rating" and "Recommended operating range"



(*1) Each lower limit value is determined by "Output voltage"- "Dropout voltage".

(*2) Operating in VCC1→VDD current path

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Electrical Characteristics at Ta = 25°C(*1), VCC1=VCC2=14.4V, V6IN=6V

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---------------------|---|------|------|-------|------|
| Quiescent current | I _{cc} | VDD w/out load, V6IN=0V, ACCIN=0V I ² C register Gr0/Gr1/Gr2=00h | | 65 | 100 | μA |
| VDD output (3.3V) | | | | | | |
| Output voltage | V _{o1} | I _{o1} =200mA | 3.13 | 3.3 | 3.47 | V |
| Output current | I _{o1} | V _{o1} ≥ 3.1V | 350 | | | mA |
| Line regulation | ΔV _{oLN1} | 5.7V<V6IN<6.5V, I _{o1} =200mA or V6IN=0V, 7.5V<VCC1<16V, I _{o1} =200mA | | 30 | 90 | mV |
| Load regulation | ΔV _{oLD1} | 1 mA<I _{o1} <200mA | | 70 | 150 | mV |
| Dropout voltage1 | V _{DROP1} | I _{o1} =200mA, V6IN=0V (applicable to VCC1→VDD) | | 0.5 | 1.0 | V |
| Dropout voltage2 | V _{DROP12} | I _{o1} =200mA (applicable to V6IN→VDD, design target) | | 1.1 | 1.3 | V |
| Ripple rejection(*2) | R _{REJ1} | f=120Hz, V6IN or VCC1=0.5Vpp I _{o1} =200mA | 40 | 50 | | dB |
| V6IN detection voltage | V6det | V6IN rising, VCC1→V6IN switch(*3) | 4.7 | 4.85 | 5.0 | V |
| V6IN detection hysteresis | V6hys | | | 100 | | mV |
| (*3): Please use V6IN≥5.7V in the case of I _o >160mA, or output voltage may be dropped when V6IN voltage is decreased to approximately "V6IN detection voltage". | | | | | | |
| SW33V output (3.3V/5V) ; SW33_EN=1 | | | | | | |
| Output voltage1 | V _{o21} | I _{o2} =200mA, SW_V=0 | 3.13 | 3.3 | 3.47 | V |
| Output voltage2 | V _{o22} | I _{o2} =200mA, SW_V=1 | 4.75 | 5.0 | 5.25 | V |
| Output current | I _{o2} | V _{o21} ≥3.1V, V _{o22} ≥4.7V | 450 | | | mA |
| Line regulation | ΔV _{oLN2} | 5.7V<V6IN<6.5V, I _{o2} =200mA | | 30 | 90 | mV |
| Load regulation | ΔV _{oLD2} | 1 mA<I _{o2} <200mA | | 70 | 150 | mV |
| Dropout voltage | V _{DROP2} | I _{o2} =200mA | | 0.25 | 0.5 | V |
| Ripple rejection(*2) | R _{REJ2} | f=120Hz, V6IN or VCC1=0.5Vpp I _{o2} =200mA | 40 | 50 | | dB |
| ILM output (5-12V); ILM_EN=1 | | | | | | |
| Output voltage1 | V _{o31} | I _{o3} =200mA, ILM_V[1:0]=00 | 4.75 | 5.0 | 5.25 | V |
| Output voltage2 | V _{o32} | I _{o3} =200mA, ILM_V[1:0]=01 | 7.6 | 8.0 | 8.4 | V |
| Output voltage3 | V _{o33} | I _{o3} =200mA, ILM_V[1:0]=10 | 9.97 | 10.5 | 11.03 | V |
| Output voltage4 | V _{o34} | I _{o3} =200mA, ILM_V[1:0]=11 | 11.4 | 12 | 12.6 | V |
| Output current | I _{o3} | | 300 | | | mA |
| Line regulation | ΔV _{oLN3} | V _o +2V<VCC2<16V, I _{o3} =200mA | | 30 | 90 | mV |
| Load regulation | ΔV _{oLD3} | 1 mA<I _{o3} <200mA | | 70 | 150 | mV |
| Dropout voltage1 | V _{DROP3} | I _{o3} =200mA | | 0.6 | 1.05 | V |
| Dropout voltage2 | V _{DROP3'} | I _{o3} =100mA | | 0.3 | 0.53 | V |
| Ripple rejection(*2) | R _{REJ3} | f=120Hz, I _{o3} =200mA | 40 | 50 | | dB |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---------------------|------------------------------|----------|----------|-------|------|
| CD output (5-8V); CD_EN=1 | | | | | | |
| Output voltage1 | Vo41 | Io4=1000 mA, CD_V[1:0]=00 | 4.75 | 5.0 | 5.25 | V |
| Output voltage2 | Vo42 | Io4=1000 mA, CD_V[1:0]=01 | 5.7 | 6.0 | 6.3 | V |
| Output voltage3 | Vo43 | Io4=1000 mA, CD_V[1:0]=10 | 6.65 | 7.0 | 7.35 | V |
| Output voltage4 | Vo44 | Io4=1000 mA, CD_V[1:0]=11 | 7.6 | 8.0 | 8.4 | V |
| Output current | Io4 | Vo41≥4.7V, V44≥7.6V | 1300 | | | mA |
| Line regulation | ΔV_{oLN4} | Vo+2V<Vcc2<16V, Io4=1000mA | | 50 | 100 | mV |
| Load regulation | ΔV_{oLD4} | 10mA<Io4<1000mA | | 100 | 200 | mV |
| Dropout voltage1 | V _{DROP4} | Io4=1000mA | | 0.9 | 1.5 | V |
| Dropout voltage2 | V _{DROP4'} | Io4=500mA | | 0.45 | 0.75 | V |
| Ripple rejection(*2) | R _{REJ4} | f=120Hz, Io4=1000mA | 40 | 50 | | dB |
| AUDIO output (5-11.5V); AUDIO_EN=1 | | | | | | |
| Output voltage1 | Vo51 | Io5=150mA, AUD_V[1:0]=00 | 4.75 | 5.0 | 5.25 | V |
| Output voltage2 | Vo52 | Io5=150mA, AUD_V[1:0]=01 | 8.13 | 8.5 | 8.87 | V |
| Output voltage3 | Vo53 | Io5=150mA, AUD_V[1:0]=10 | 8.55 | 9.0 | 9.45 | V |
| Output voltage4 | Vo54 | Io5=150mA, AUD_V[1:0]=11 | 10.9 | 11.5 | 12.08 | V |
| Output current | Io5 | | 250 | | | mA |
| Line regulation | ΔV_{oLN5} | Vo+1V<VCC2<16V, Io5=150mA | | 30 | 90 | mV |
| Load regulation | ΔV_{oLD5} | 1mA<Io5<150mA | | 70 | 150 | mV |
| Dropout voltage | V _{DROP5} | Io5=150mA | | 0.25 | 0.45 | V |
| Ripple rejection(*2) | R _{REJ5} | f=120Hz, Io5=150mA | 40 | 50 | | dB |
| EXT_HS-SW; EXT_EN=1 | | | | | | |
| Output voltage | Vo6 | Io6=350mA | Vcc2-1.0 | Vcc2-0.5 | | V |
| Output current | Io6 | Vo6≥VCC2-1.0 | 350 | | | mA |
| ANT_HS-SW; ANT_EN=1 | | | | | | |
| Output voltage | Vo7 | Io7=300mA | Vcc2-1.0 | Vcc2-0.5 | | V |
| Output current | Io7 | Vo7≥VCC2-1.0 | 300 | | | mA |
| ACC detection | | | | | | |
| Detection voltage1 | Vacc1 | ACC_V[1:0]=00, ACCIN falling | 2.62 | 2.7 | 2.78 | V |
| Detection voltage 2 | Vacc2 | ACC_V[1:0]=01, ACCIN falling | 3.1 | 3.2 | 3.3 | V |
| Detection voltage 3 | Vacc3 | ACC_V[1:0]=10, ACCIN falling | 3.49 | 3.6 | 3.71 | V |
| Detection voltage 4 | Vacc4 | ACC_V[1:0]=11, ACCIN falling | 4.07 | 4.2 | 4.33 | V |
| Release voltage1 | Vaccr1 | ACC_V[1:0]=00, ACCIN rising | 2.81 | 2.9 | 2.99 | V |
| Release voltage 2 | Vaccr2 | ACC_V[1:0]=01, ACCIN rising | 3.3 | 3.4 | 3.5 | V |
| Release voltage 3 | Vaccr3 | ACC_V[1:0]=10, ACCIN rising | 3.68 | 3.8 | 3.92 | V |
| Release voltage 4 | Vaccr4 | ACC_V[1:0]=11, ACCIN rising | 4.26 | 4.4 | 4.54 | V |
| Threshold hysteresis | Vachs | | | 0.2 | | V |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------|-----------------------------------|------|---------|------|------|
| Under-Voltage detection(UVDET) | | | | | | |
| detection voltage1 | Vuv1 | VCC2 falling, UVD_V[1:0]=00 | 5.82 | 6.0 | 6.18 | V |
| detection voltage2 | Vuv2 | VCC2 falling, UVD_V[1:0]=01 | 6.79 | 7.0 | 7.21 | V |
| detection voltage3 | Vuv3 | VCC2 falling, UVD_V[1:0]=10 | 7.56 | 7.8 | 8.04 | V |
| detection voltage4 | Vuv4 | VCC2 falling, UVD_V[1:0]=11 | 8.73 | 9.0 | 9.27 | V |
| release voltage1 | Vuvr1 | VCC2 rising, UVD_V[1:0]=00 | 6.06 | 6.25 | 6.43 | V |
| release voltage2 | Vuvr2 | VCC2 rising, UVD_V[1:0]=01 | 7.13 | 7.35 | 7.57 | V |
| release voltage3 | Vuvr3 | VCC2 rising, UVD_V[1:0]=10 | 8.05 | 8.3 | 8.55 | V |
| release voltage4 | Vuvr4 | VCC2 rising, UVD_V[1:0]=11 | 9.40 | 9.7 | 9.99 | V |
| detection hysteresis1 | Vuvhs1 | UVD_V[1:0]=00 | | 0.25 | | V |
| detection hysteresis2 | Vuvhs2 | UVD_V[1:0]=01 | | 0.35 | | V |
| detection hysteresis3 | Vuvhs3 | UVD_V[1:0]=10 | | 0.5 | | V |
| detection hysteresis4 | Vuvhs4 | UVD_V[1:0]=11 | | 0.7 | | V |
| Over-Voltage detection(OVDET) | | | | | | |
| detection voltage | Vovd | VCC2 rising | 17 | 18 | 19 | V |
| detection hysteresis | Vodhys | | | 0.5 | | V |
| Over-Voltage protection(OVP) | | | | | | |
| detection voltage | Vovp | VCC1/VCC2 rising, output disabled | | 23 | | V |
| detection hysteresis | Vovhys | | | 0.5 | | V |
| V6IN Shutdown detection(V6SDN) | | | | | | |
| detection voltage | V6sdn | V6IN falling, output disabled | 0.6 | 1.02 | 1.4 | V |
| detection hysteresis | V6sdhs | | | 80 | | mV |
| FLG output | | | | | | |
| FLG "H" voltage | VflgH | Isource=1mA | | VDD-0.3 | VDD | V |
| FLG "L" voltage | VflgL | Isink=1mA | | 0.3 | 0.4 | V |
| I²C-BUS I/F; SCL,SDA | | | | | | |
| Input "L" voltage | V _{IL} | | 0 | | 0.4 | V |
| Input "H" voltage | V _{IH} | | 2.8 | 3.3 | 5.5 | V |
| SDA "L" voltage | V _{OL} | Isink=1mA, ACK or data read | | 0.3 | 0.4 | V |

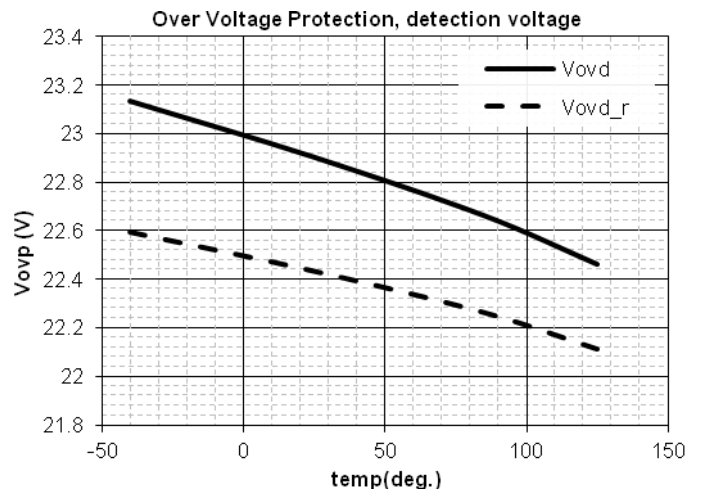
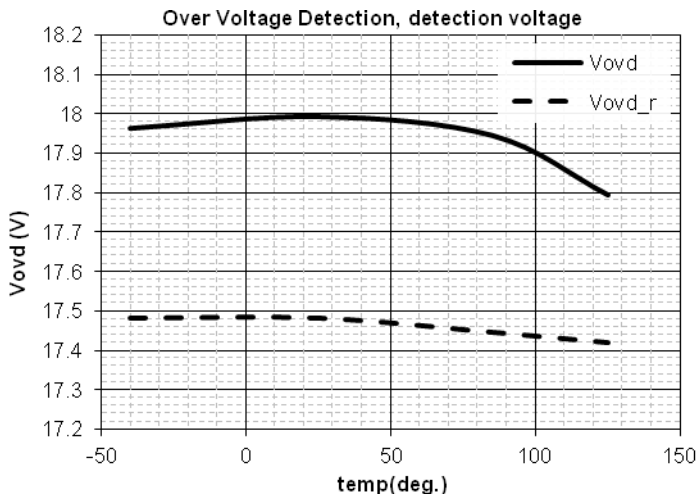
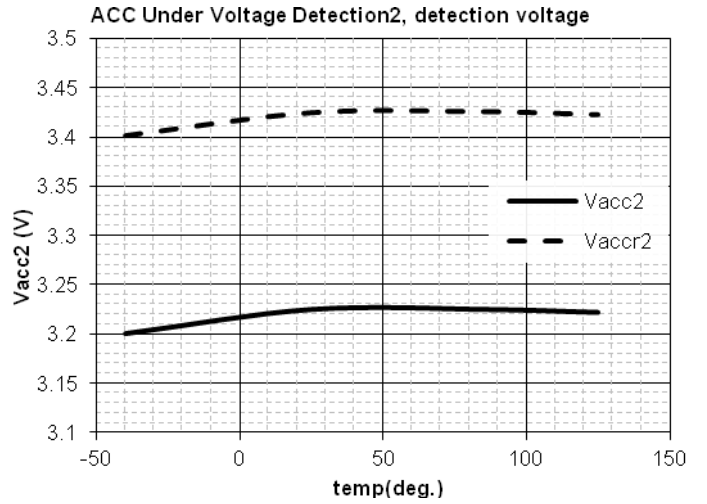
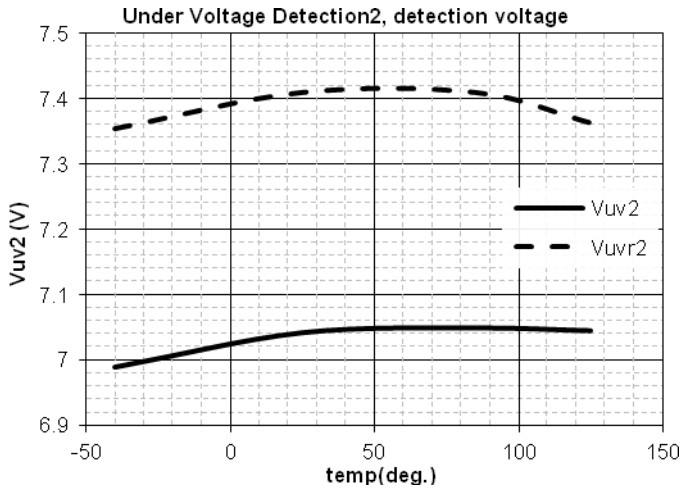
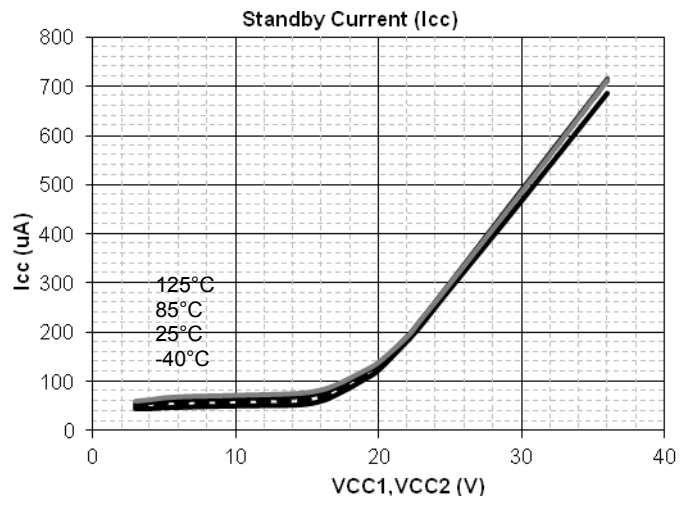
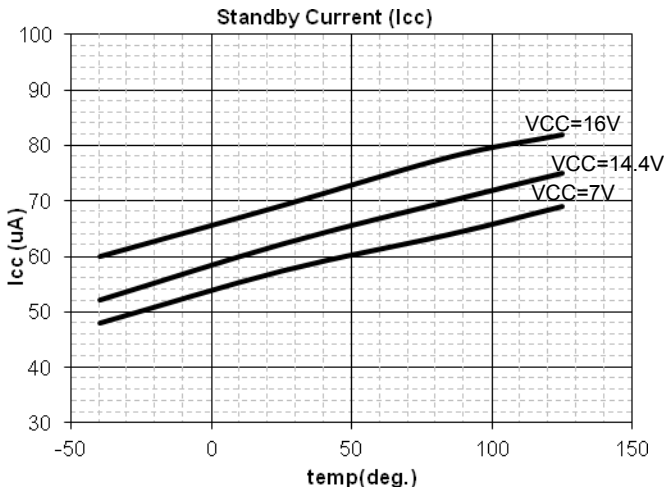
(*1) All the specification is defined based on the tests performed under the conditions where T_j and T_a(=25°C) are almost equal. These tests were performed with pulse load to minimize the increase of junction temperature (T_j).

(*2) guaranteed by design

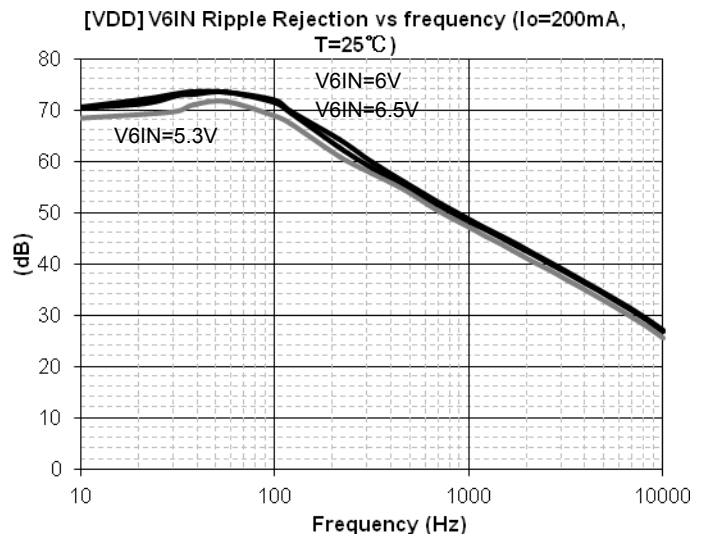
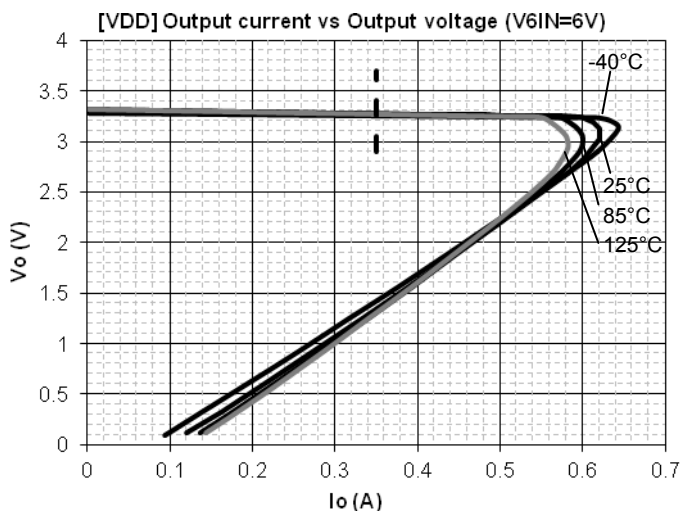
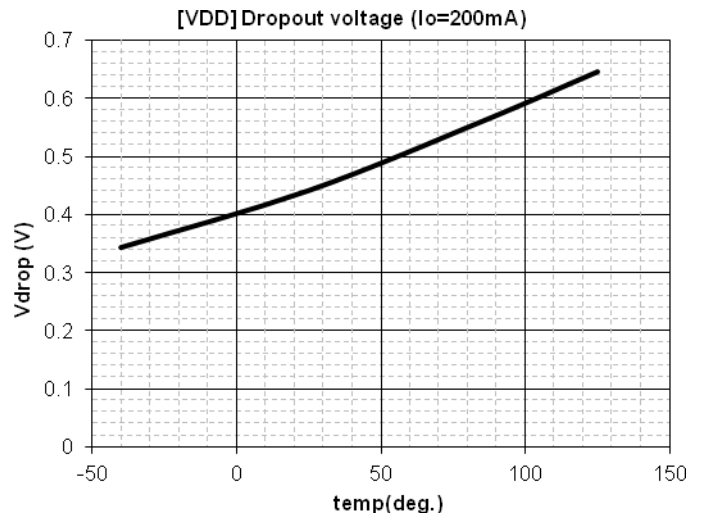
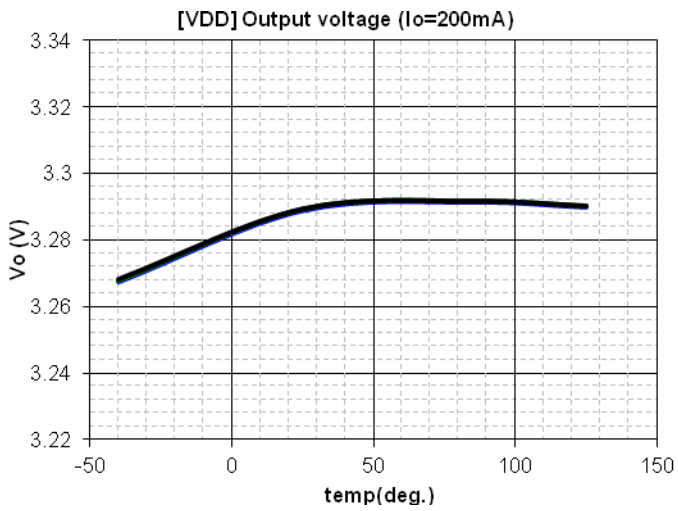
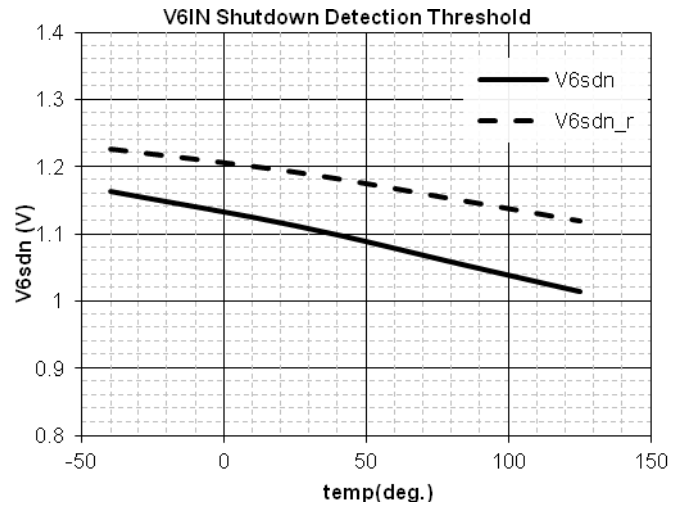
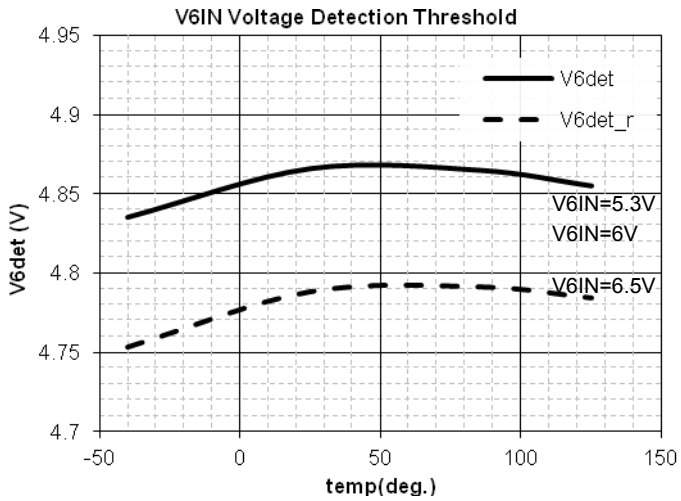
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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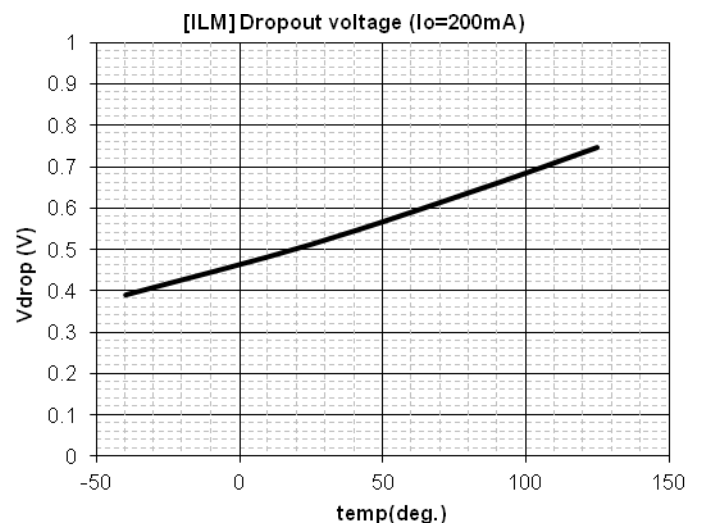
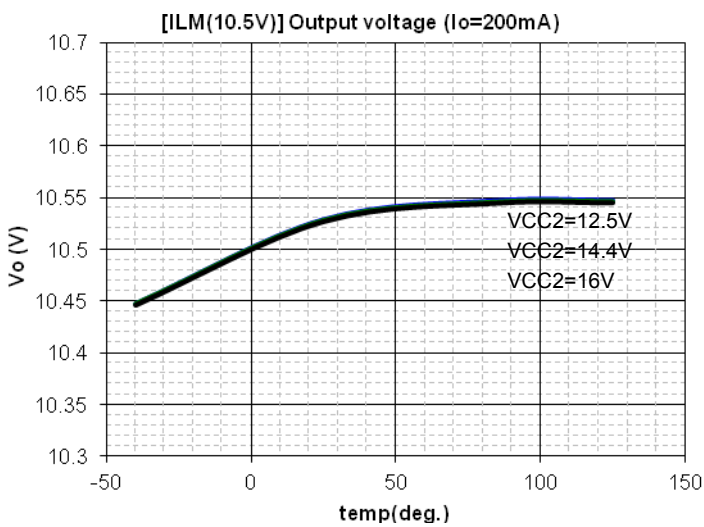
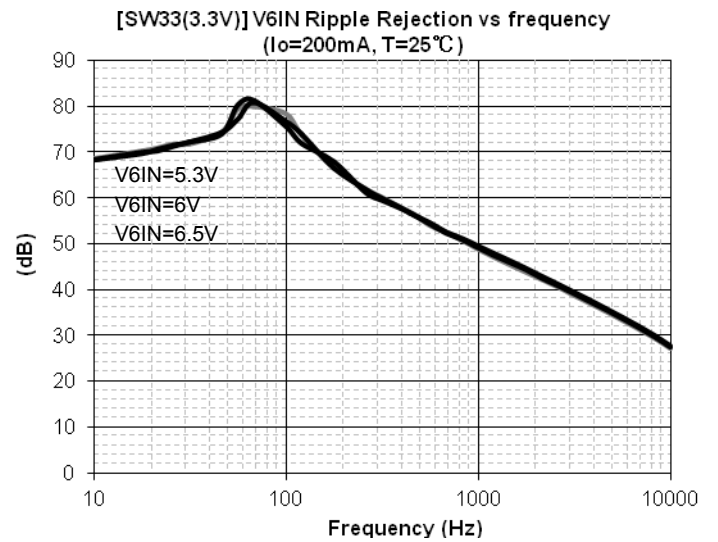
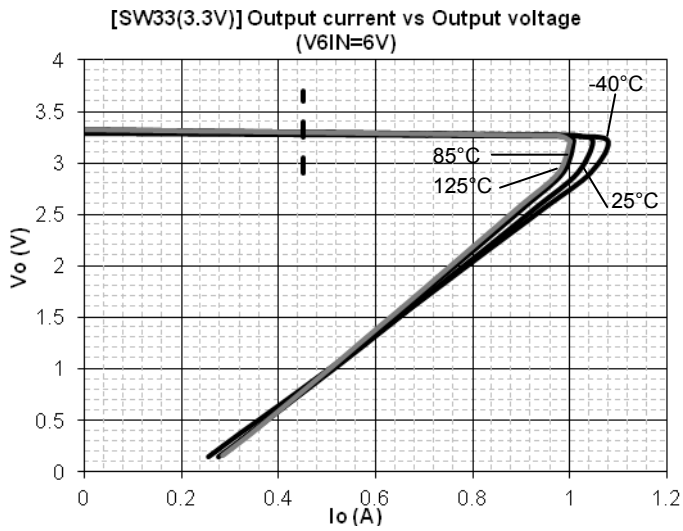
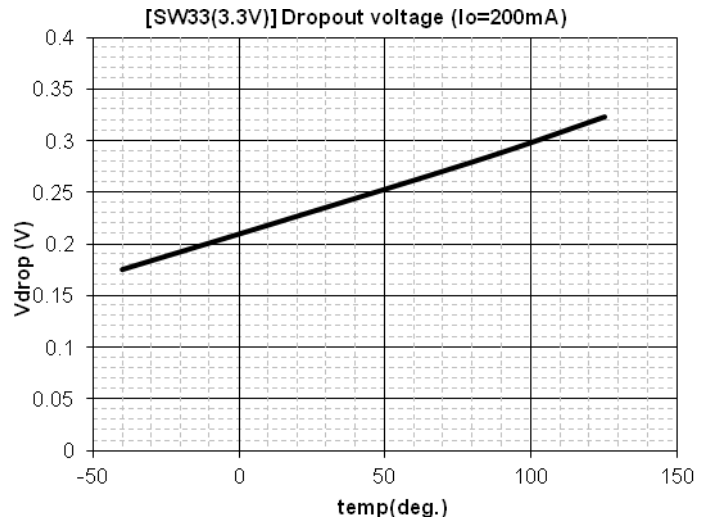
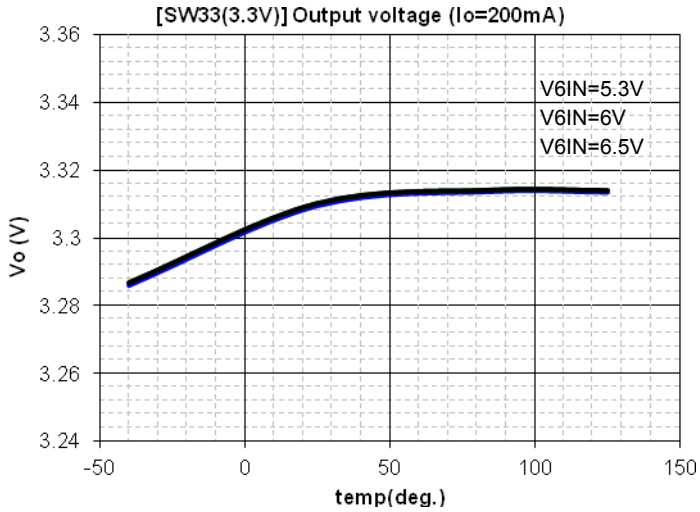
TYPICAL CHARACTERISTICS



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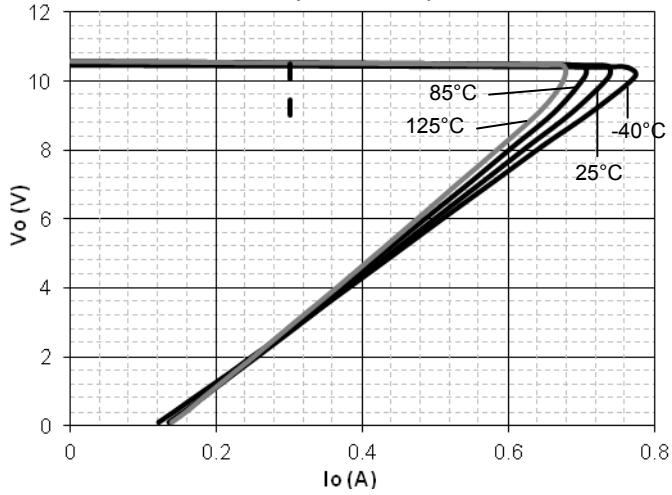


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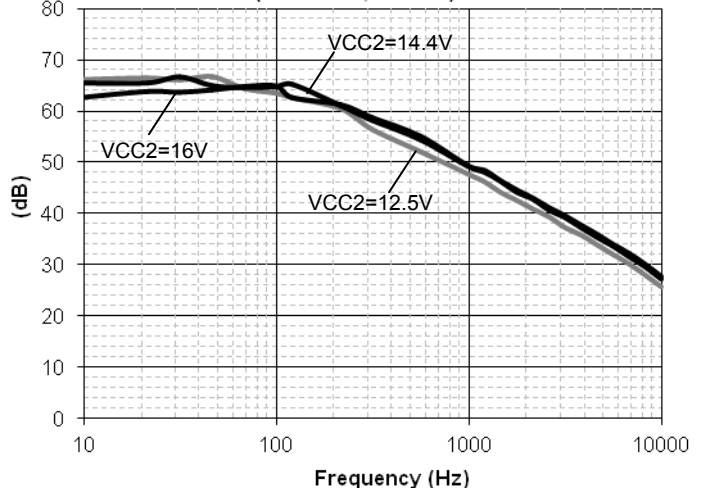


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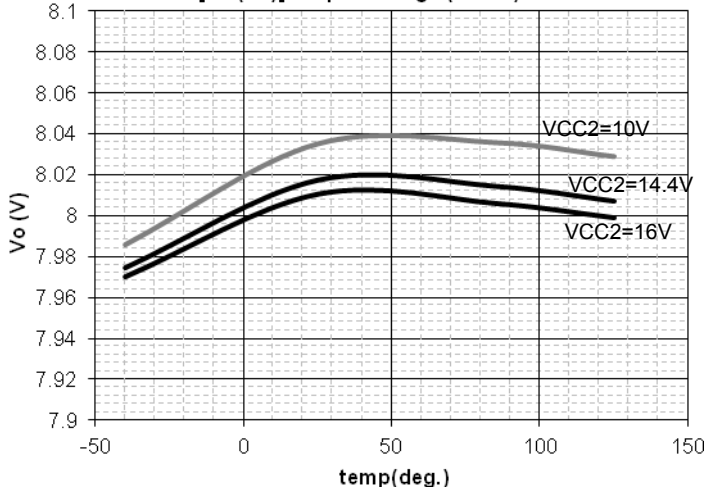
[ILM(10.5V)] Output current vs Output voltage
(VCC2=14.4V)



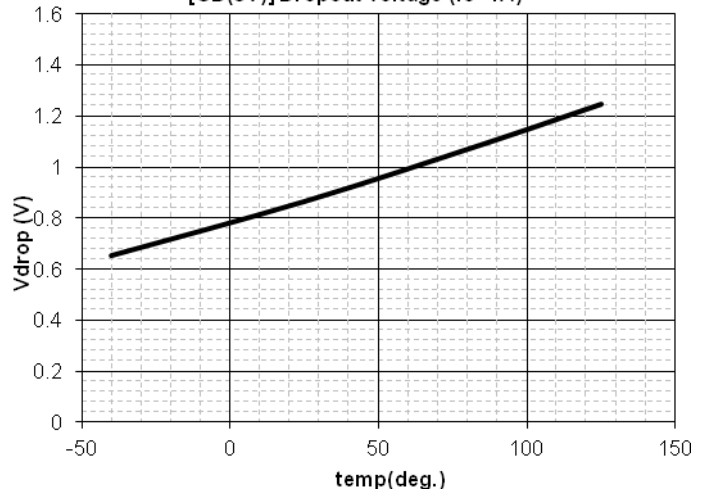
[ILM(10.5V)] Ripple Rejection vs frequency
(Io=200mA, T=25°C)



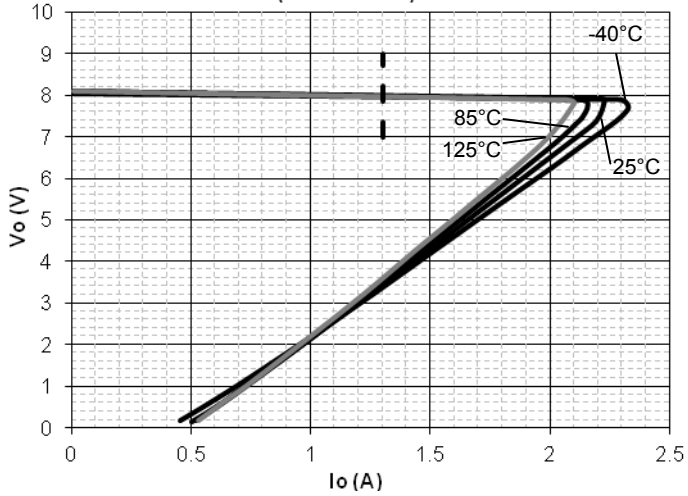
[CD(8V)] Output voltage (Io=1A)



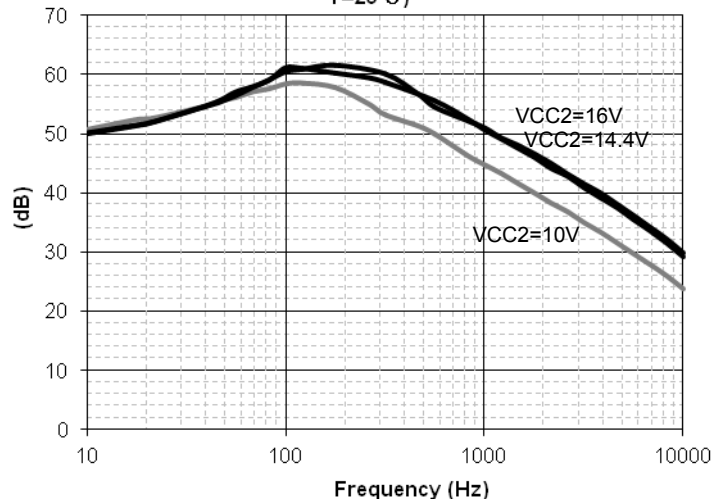
[CD(8V)] Dropout voltage (Io=1A)



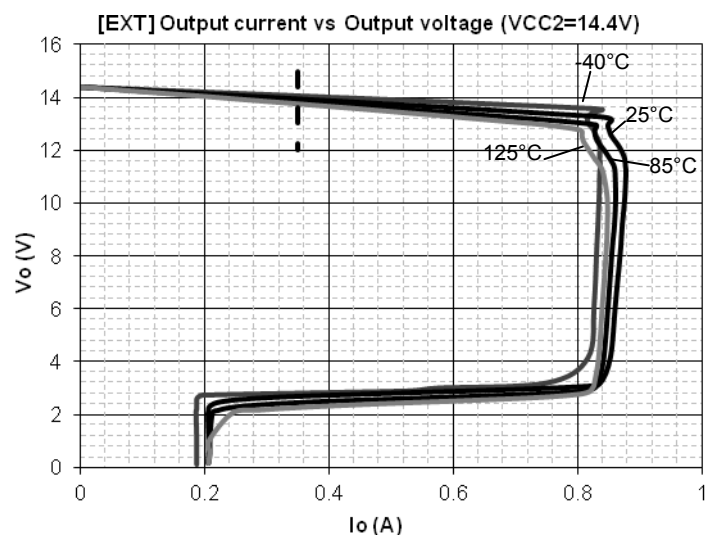
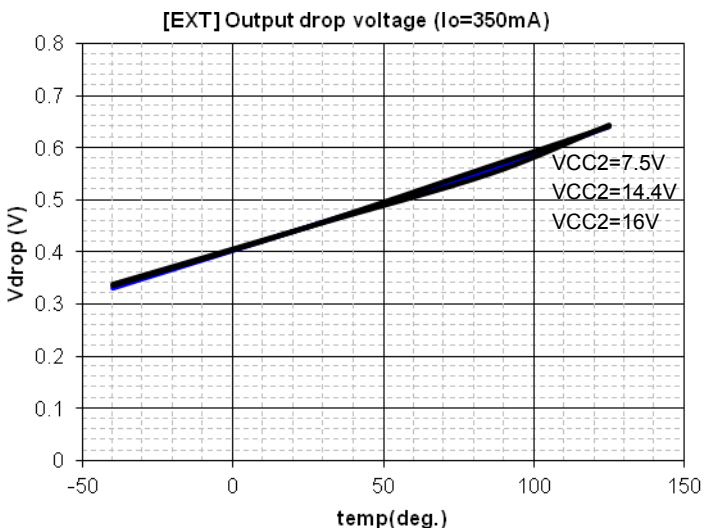
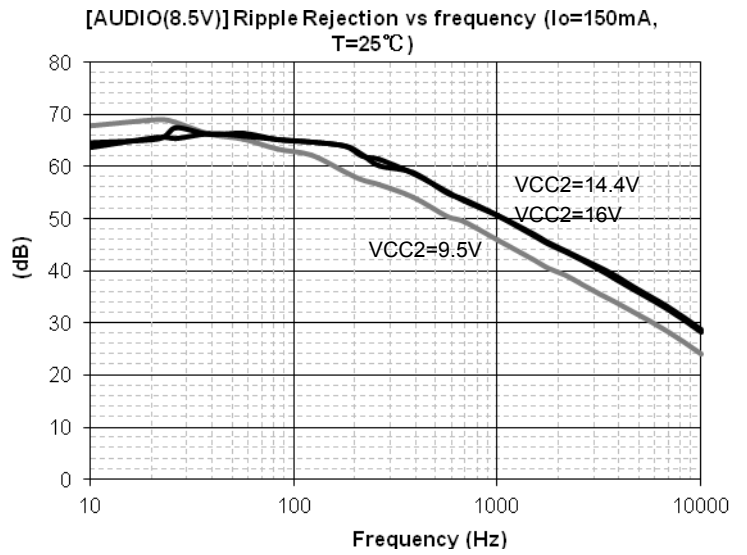
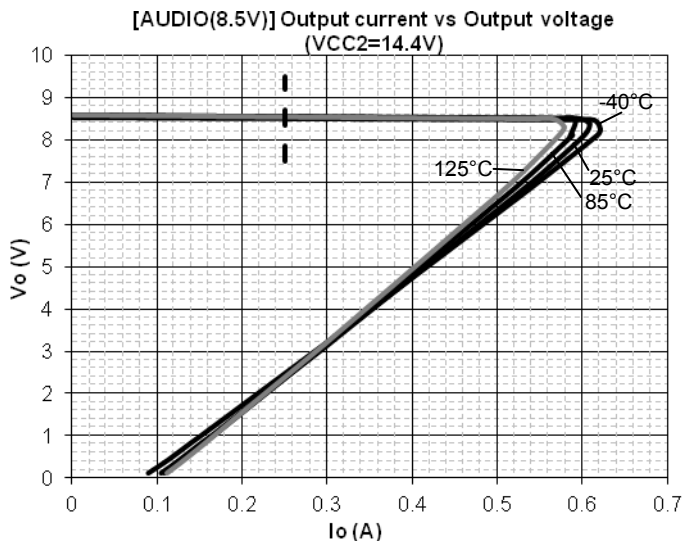
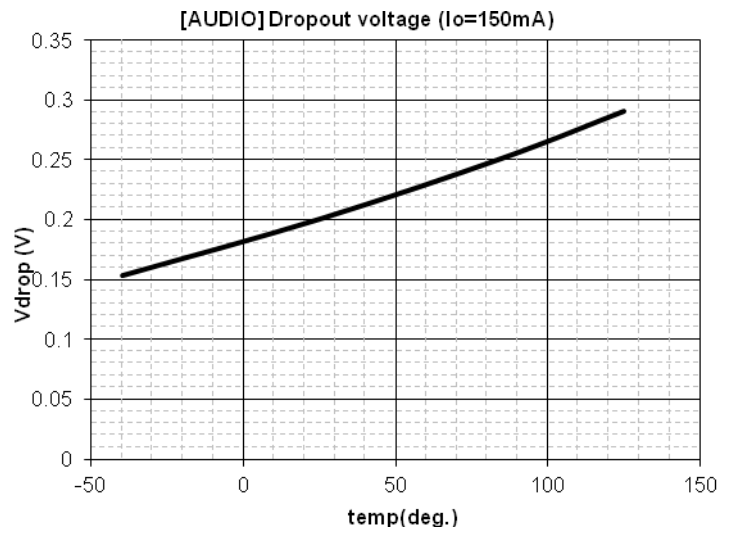
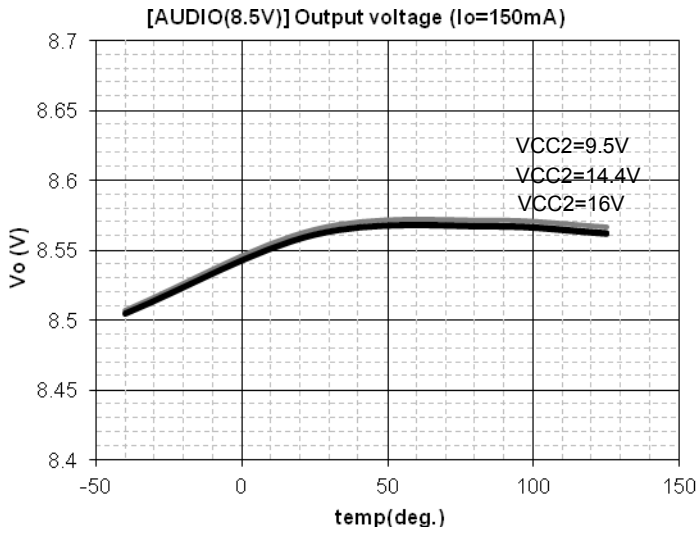
[CD(8V)] Output current vs Output voltage
(VCC2=14.4V)



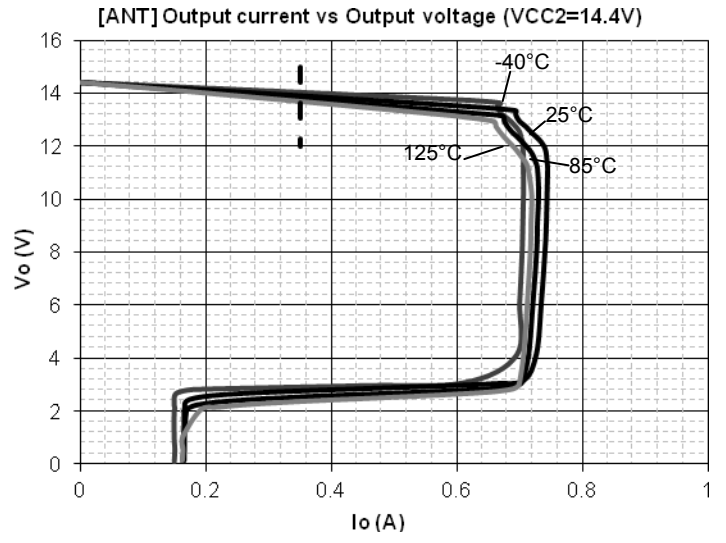
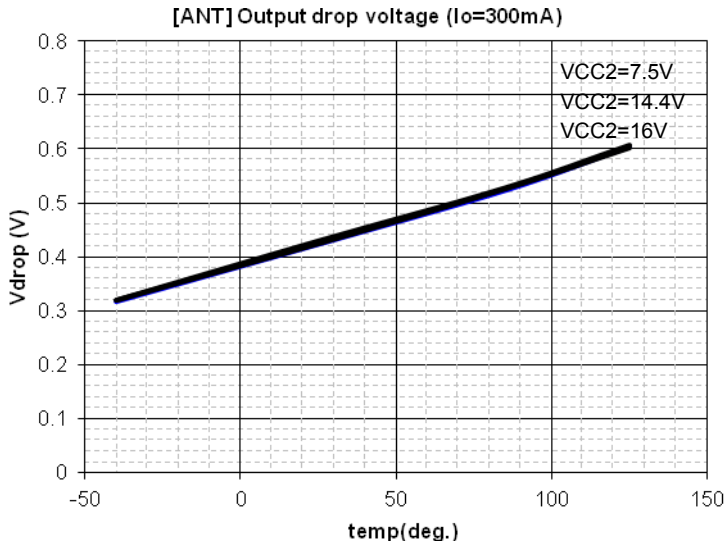
[CD(8V)] Ripple Rejection vs frequency (Io=1000mA, T=25°C)



LV5685PV

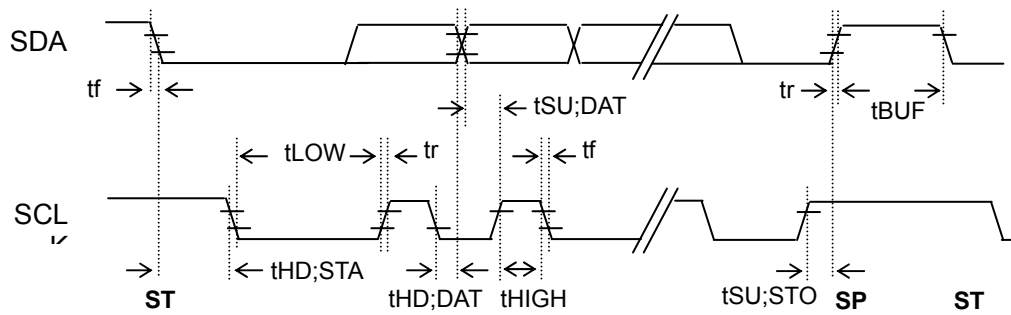


LV5685PV



I²C-bus Interface timing

| Parameter | Symbol | min | typ | max | unit |
|---|---------|-----|-----|-----|------|
| SCL clock frequency | fSCL | 0 | | 400 | kHz |
| START condition hold time | tHD;STA | 0.6 | | | us |
| SCL "L" pulse-width | tLOW | 1.3 | | | us |
| SCL "H" pulse-width | tHIGH | 0.6 | | | us |
| DATA hold time | tHD;DAT | 0 | | | us |
| DATA setup time | tSU;DAT | 0.1 | | | us |
| SDA/SCL rise time | tr | | | 0.3 | us |
| SDA/SCL fall time | tf | | | 0.3 | us |
| STOP condition setup time | tSU;STO | 0.6 | | | us |
| Bus free time between STOP and START condition | tBUF | 1.3 | | | us |
| Bus line load capacitance | Cb | | | 400 | pF |



I²C bus interface format (MSB first)

This part is I²C controlled power supply, using 2 wires of SCL,SDA.

The communication protocol comprises start-condition, device-address, sub-address, data and stop-condition.

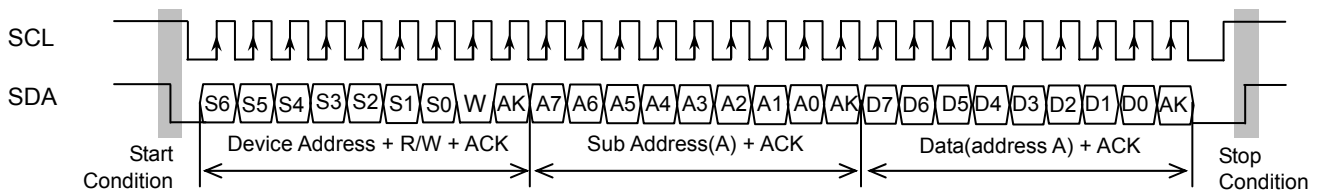
Every 8bits are followed by ACK bit, and the receiver device pulls down SDA line during ACK period.

This part doesn't accept sub-address auto increment format. (Single data byte write per a communication.)

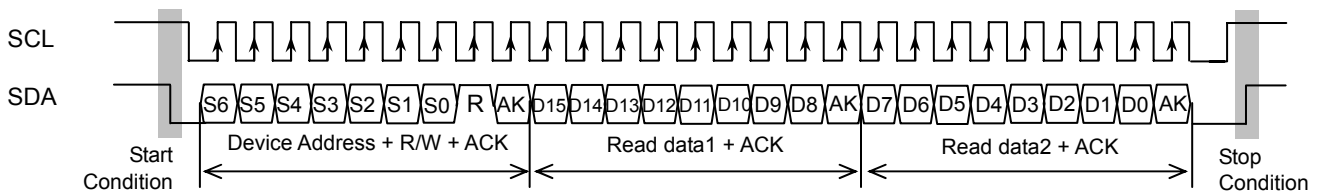
The protocol in Read-mode comprises start-condition, device-address, data1, data2 and stop-condition.

(Note)The I²C-bus communication may be unstable when VDD voltage is not stable or out of specification range, since I²C-BUS circuitry is supplied by VDD.

Write mode



Read mode



• Device address

| | | | | | | | |
|----|----|----|----|----|----|----|-----|
| S6 | S5 | S4 | S3 | S2 | S1 | S0 | R/W |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 |

• Register map

Write

| | | | | | | | | | |
|------|--------|--------|----------|---------|--------|--------|------|----|----------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | init |
| PM | ILM_EN | CD_EN | AUDIO_EN | SW33_EN | EXT_EN | ANT_EN | | | 00000000 |
| VCTL | ILM_V1 | ILM_V0 | CD_V1 | CD_V0 | AUD_V1 | AUD_V0 | SW_V | | 00000000 |
| DET | ACC_V1 | ACC_V0 | UVD_V1 | UVD_V0 | FLGMD1 | FLGMD0 | | | 00000000 |

Read

| | | | | | | | | | |
|------|--------|--------|-------|-------|--------|--------|------|-------|----------|
| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | init |
| VCTL | ILM_V1 | ILM_V0 | CD_V1 | CD_V0 | AUD_V1 | AUD_V0 | SW_V | V6DET | 00000000 |

| | | | | | | | | | |
|-----|-------|----|----|-----|-------|----|----|----|----------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | init |
| FLG | ACCUV | UV | OV | OVP | V6SDN | OC | 0 | 0 | 00000000 |

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Write Register explanation

| ADR | bit | Name | init | Description |
|-----|-----|----------|------|----------------------------------|
| 00h | 7 | ILM_EN | 0 | ILM output enable 1: ON 0: OFF |
| | 6 | CD_EN | 0 | CD output enable 1: ON 0: OFF |
| | 5 | AUDIO_EN | 0 | AUDIO output enable 1: ON 0: OFF |
| | 4 | SW33_EN | 0 | SW33 output enable 1: ON 0: OFF |
| | 3 | EXT_EN | 0 | EXT output enable 1: ON 0: OFF |
| | 2 | ANT_EN | 0 | ANT output enable 1: ON 0: OFF |
| | 1 | | 0 | |
| | 0 | | 0 | |

| ADR | bit | Name | init | Description |
|-----|-------|------------|------|--|
| 01h | [7:6] | ILM_V[1:0] | 00 | ILM output voltage(*) 11: 12V 10: 10.5V 01: 8V 00: 5V |
| | [5:4] | CD_V[1:0] | 00 | CD output voltage(*) 11: 8V 10: 7V 01: 6V 00: 5V |
| | [3:2] | AUD_V[1:0] | 00 | AUDIO output voltage(*) 11: 11.5V 10: 9V 01: 8.5V 00: 5V |
| | 1 | SW_V | 0 | SW33V output voltage(*) 1: 5V 0: 3.3V |
| | 0 | | 0 | |

(*) "Output voltage setting" is only valid when corresponding output is set disabled(xxx_EN=0). It is ignored when the output is set enabled(xxx_EN=1).

| ADR | bit | Name | init | Description |
|-----|-------|------------|------|---|
| 02h | [7:6] | ACC_V[1:0] | 00 | ACC detection voltage 11: 4.2V 10: 3.6V 01: 3.2V 00: 2.7V |
| | [5:4] | UVD_V[1:0] | 00 | UVDET detection voltage 11: 9V 10: 7.8V 01: 7V 00: 6V |
| | [3:2] | FLGMD[1:0] | 00 | FLG output mode 11/10: BDET only 01: ACC only, 00: ACC/BDET |
| | 1 | | 0 | |
| | 0 | | 0 | |

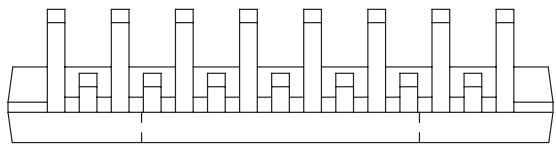
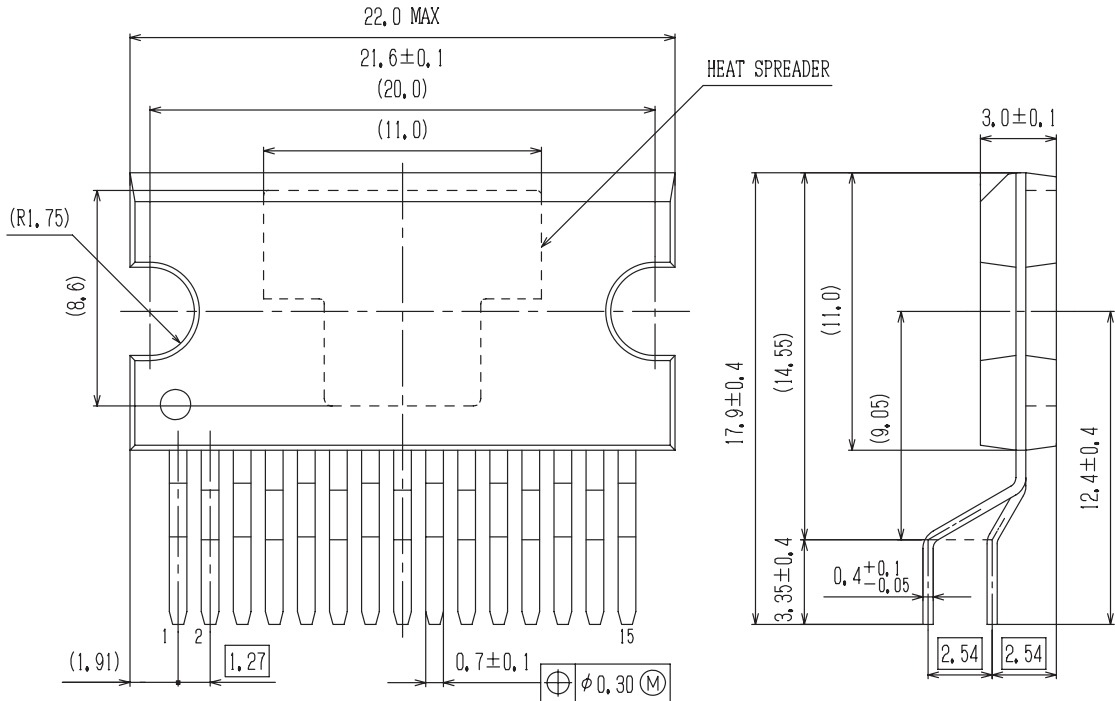
Read Register explanation

| ADR | bit | Name | init | Description |
|-----|---------|------------|------|--|
| | [15:14] | ILM_V[1:0] | 00 | ILM output voltage 11: 12V 10: 10.5V 01: 8V 00: 5V |
| | [13:12] | CD_V[1:0] | 00 | CD output voltage 11: 8V 10: 7V 01: 6V 00: 5V |
| | [11:10] | AUD_V[1:0] | 00 | AUDIO output voltage 11: 11.5V 10: 9V 01: 8.5V 00: 5V |
| | 9 | SW_V | 0 | SW33V output voltage 1: 5V 0: 3.3V |
| | 8 | V6DET | 0 | V6INDET / Supply for VDD 1: V6IN 0: VCC1 |
| | 7 | ACCUV | 0 | ACC detection 1: Under voltage 0: Normal |
| | 6 | UV | 0 | Under voltage detection 1: Under voltage 0: Normal |
| | 5 | OV | 0 | Over voltage detection 1: Over Voltage 0: Normal |
| | 4 | OVP | 0 | Over voltage protection 1: Over Voltage Protection 0: Normal |
| | 3 | V6SDN | 0 | V6IN shutdown detection 1: V6IN shutdown 0: V6IN applied |
| | 2 | OC | 0 | Output Over Current 1: Over current 0: Normal |
| | 1 | | 0 | |
| | 0 | | 0 | |

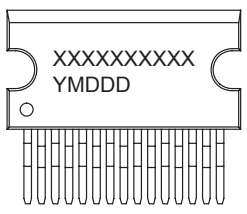
Package Dimensions

unit : mm

HZIP15
CASE 945AB
ISSUE A



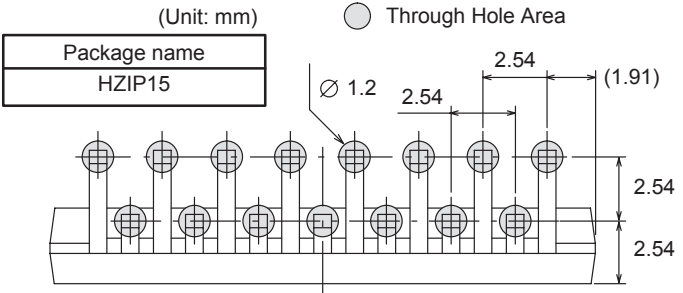
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

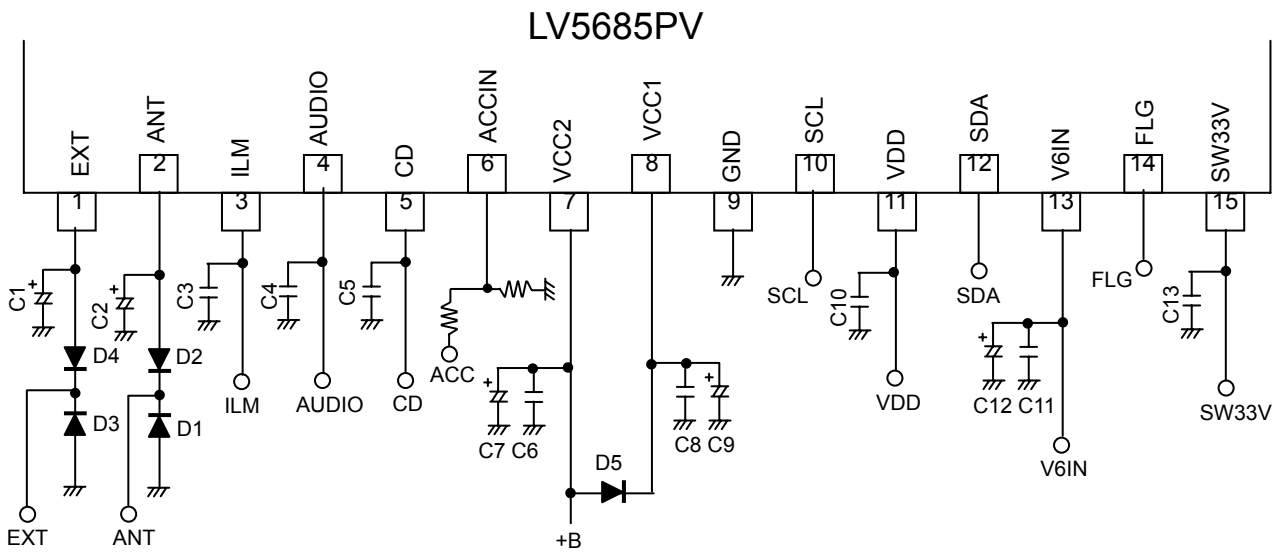
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Application Circuit Example



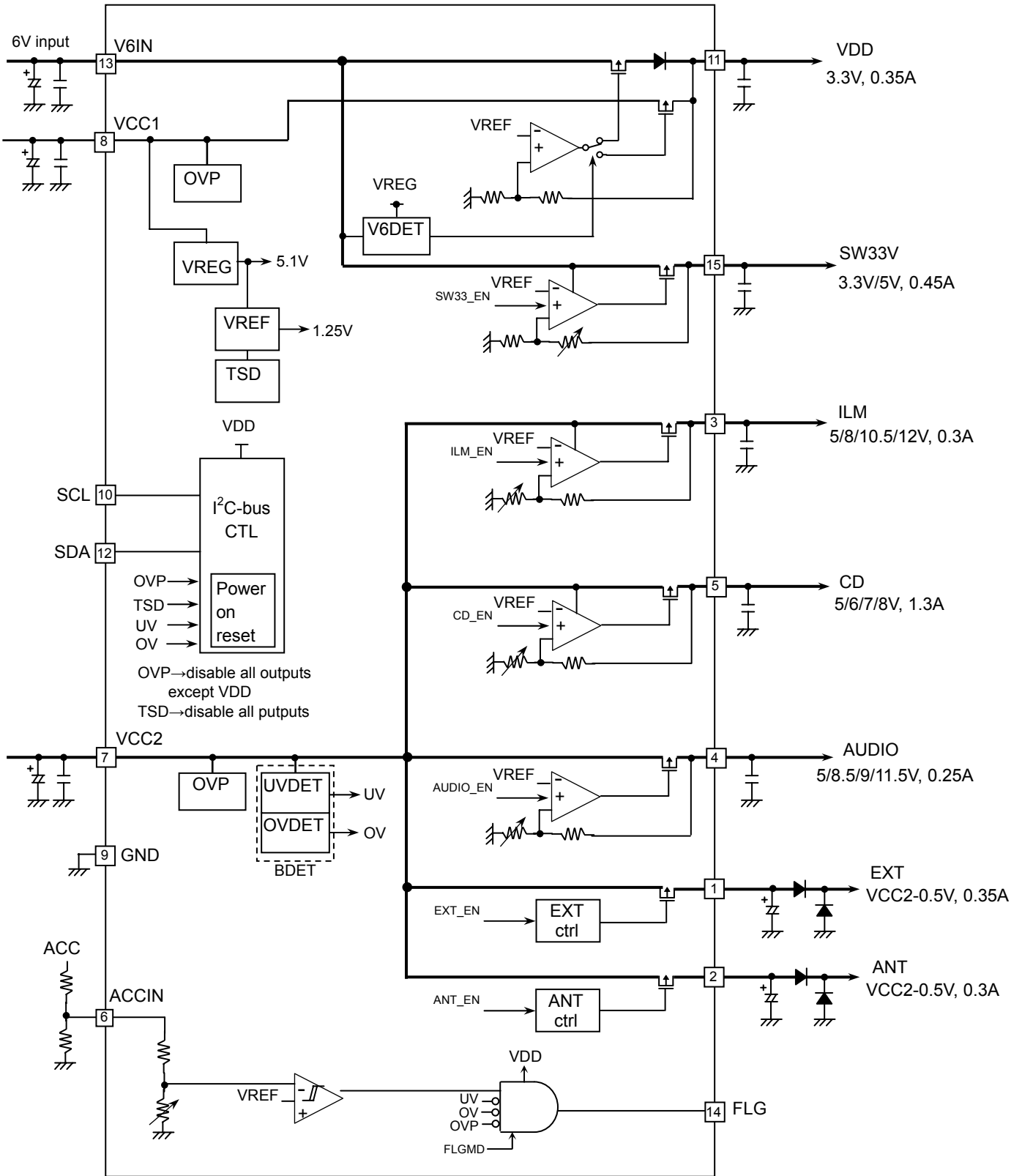
■Peripheral parts

| Part name | Description | Recommended value | Note |
|----------------------|--|---|--|
| C1,C2 | Capacitor for EXT/ANT output stabilization | greater than 2.2 μ F | |
| C3,C4,C5, C10,C13 | output stabilization capacitor | greater than 10 μ F(*1) | |
| C7,C9,C12 | Capacitor for bypass power supply | C7: greater than 100 μ F C9,C12: greater than 47 μ F | Make sure to implement close to VCC and GND. |
| C6,C8,C11 | Capacitor for oscillation protector | greater than 0.22 μ F | |
| D1,D2,D3,D4 | Internal device protection diode | ON Semiconductor SB1003M3 | |
| D5 | Reverse current protection diode | ON Semiconductor SB1003M3 | |

(*1) Make sure that output capacitors are greater than 10 μ F and meets the condition of ESR=0.001 to 10 Ω , in which voltage/temperature dependence and unit differences are taken into consideration. Moreover, in case of electrolytic capacitor, high-frequency characteristics should be sufficiently good.

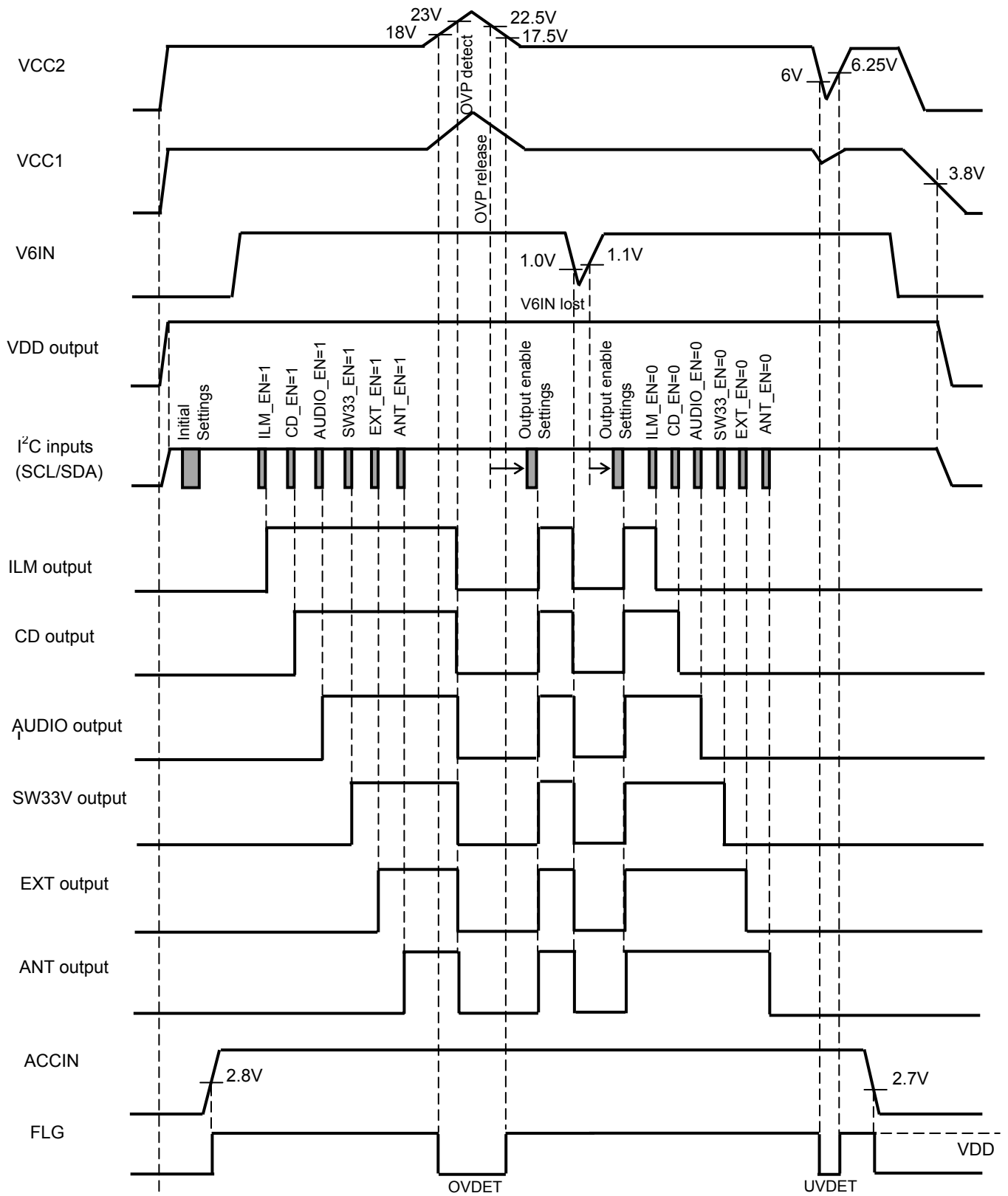
LV5685PV

Block Diagram



LV5685PV

■ Timing Chart



Note: The above values are obtained when typ. All the voltage setting are default values

Functional Description

[Standby mode]

When VCC1 is applied, internal control circuitry is automatically reset and goes into Stand-by mode.

In Stand-by mode, following functions are active.

VDD(3.3V) output

I²C-bus communication (except for "PM" register)

Over voltage protection(OVP)/UVDET/OVDET/ACC detection/FLG output

Thermal shutdown(TSD)

[VCC1/VCC2/V6IN]

VCC1 supplies VDD and common circuitry such as reference voltage, internal control circuitry. So VCC1 input is necessary for any operation of this device.

VCC2 is the supply for AUDIO/ILM/CD/EXT/ANT outputs.

LV5685PV has the tolerance value of 50V against VCC1/2 and ACCIN peak surge voltage, but for more safety set design, adding power clamp, such as power zener diode, on battery connected line is recommended in order to absorb applied surge.

LV5685PV has no protection against battery reverse connection, so adding Schottky diode is recommended to prevent a negative voltage.

V6IN is the supply for SW33V. V6IN also supplies VDD when V6IN voltage exceeds 4.85V(typ).

When VCC2 and V6IN is applied, ILM/CD/AUDIO/SW33/EXT/ANT output can be set enable via I²C-bus.

When V6IN is lower than 1.1V(typ)(max:1.5V), output enable command above can't be accepted.

[Controls]

The functions of LV5685PV can be controlled via I2C bus. See "I2C bus interface format" term for details.

[Linear Regulators]

VDD output

When VCC1 is applied, VDD output is active regardless of control states. When V6IN is applied and the voltage exceeds 4.85V(typ), supply for VDD output switches from VCC1 to V6IN in order to reduce power dissipation.

See "VDD regulator circuit description" term for detail.

SW33V/CD/AUDIO/ILM output

These outputs are individually enabled or disabled via I²C-bus.

The voltage of each output can be selected via I²C-bus. These commands must be set prior to enabling corresponding output. If you change the voltage for these outputs, be sure to do it after the output is set disabled. In order to avoid unwanted output voltage change, each "output voltage setting" is accepted only when corresponding output is set disabled(XXX_EN=0). The "output voltage setting" is ignored if the output is set enabled(XXX_EN=1).

Output voltage setting can be referred by reading via I²C-bus(VCTL register). It is strongly recommended to read and check VCTL register value just before setting enable the output in order to avoid unwanted output voltage change even in case if communication error were to happen and incorrect voltage setting were written to the device.

Each regulator output limits output current if the output gets over-loaded condition. The limit current decreases as the output voltage gets lower, in order to reduce the stress applied to the device.

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All regulators in LV5685PV are low dropout outputs, because the output stage of all regulators is P-channel LDMOS.

When you select output capacitors for linear regulators, you should consider three main characteristics: startup delay, transient response and loop stability. The capacitor values and type should be based on cost, availability, size and temperature constraints. Tantalum, Aluminum electrolytic, Film, or Ceramic capacitors are all acceptable solutions. However, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but if the circuit operates at low temperatures (-25 to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's datasheet usually provides this information.

[High-side switches]

ANT and EXT are high-side power switches connected to VCC2. These outputs are individually enabled or disabled via I²C-bus.

Each high-side switch limits output current if the output gets over-loaded condition. The limit current becomes lower value, if the output voltage gets lower than 2.5V(typ) in order to reduce the stress applied to the device. If these outputs are connected to inductive load or loads which have different ground potential, protection diodes (D1-4) are necessary to protect the device from negative voltage.

[Current Limiting]

When the each output becomes in over load condition, the device limits the output current.

All outputs are also protected against short circuit by fold back current limiter.

If one of each output except VDD is in over-current condition, OC bit of FLG register is set 1, which can be read via I²C-bus.

[FLG output]

FLG is the CMOS level logic output which indicates the combination of several detectors' results.

FLG output is set "High"(VDD voltage), if all the following conditions are satisfied.

| | Conditions | FLGMD[1:0] | | |
|------|---|------------|---------|---------|
| | | 00 | 01 | 10 or11 |
| ACC | ACC input voltage>ACC detection threshold | ✓ | ✓ | ignored |
| BDET | VCC2 voltage>UVDET threshold | ✓ | ignored | ✓ |
| | VCC2 voltage<OVDET threshold | ✓ | ignored | ✓ |
| OVP | VCC1<OVP threshold and VCC2<OVP threshold | ✓ | ignored | ✓ |
| TSD | Die temperature<175°C(typ) | ✓ | ✓ | ✓ |
| | VDD output current< Iomax | ✓ | ✓ | ✓ |

Note: I²C-bus "FLG" register bits is active regardless of FLGMD[1:0] setting.

[Detections]

Under voltage detection (UVDET)

If the VCC2 voltage gets lower than set value (UVD_V[1:0]), Under-Voltage is detected and the UV bit of FLG register is set 1, which can be read via I²C-bus. FLG pin keeps "Low" during UVDET condition except for at FLGMD[1:0]=01. Each output status keeps the same condition even if UV is detected.

Over voltage detection (OVDET)

If the VCC2 voltage exceeds 18V(typ), Over-Voltage is detected and the OV bit of FLG register is set 1, which can be read via I²C-bus. FLG pin keeps "Low" during OVDET condition except for at FLGMD[1:0]=01. Each output status keeps the same condition even if OV is detected.

ACC Under voltage detection

If the ACCIN voltage gets lower than set value (ACC_V[1:0]), the ACCUV bit of FLG register is set 1, which can be read via I²C-bus. FLG pin keeps "Low" during ACCUV is detected if FLGMD[1:0] is 00 or 01.

Each output status keeps the same condition even if ACCUV is detected.

Over voltage protection (OVP)

If the voltage of VCC1 or VCC2 exceed 23V(typ), OVP is detected and the OVP bit of FLG register is set 1, which can be read via I²C-bus. And all the outputs except VDD are automatically turned off. When the voltage of VCC1 and VCC2 get lower than 22.5V(typ), OVP detection is released. But output voltages are not automatically restored, because once OVP is detected, PM register of I²C-bus is reset.

FLG pin keeps "Low" during OVP condition except for at FLGMD[1:0]=01.

V6IN shutdown detection

If the V6IN voltage decreases lower than 1.0V(typ), V6IN-shutdown is detected and the V6SDN bit of FLG register is set 1, which can be read via I²C-bus. And all the outputs except VDD are automatically turned off. Output voltages are not automatically activated if V6IN voltage is restored, because once V6IN shutdown is detected, PM register of I²C-bus is reset.

Thermal Shutdown

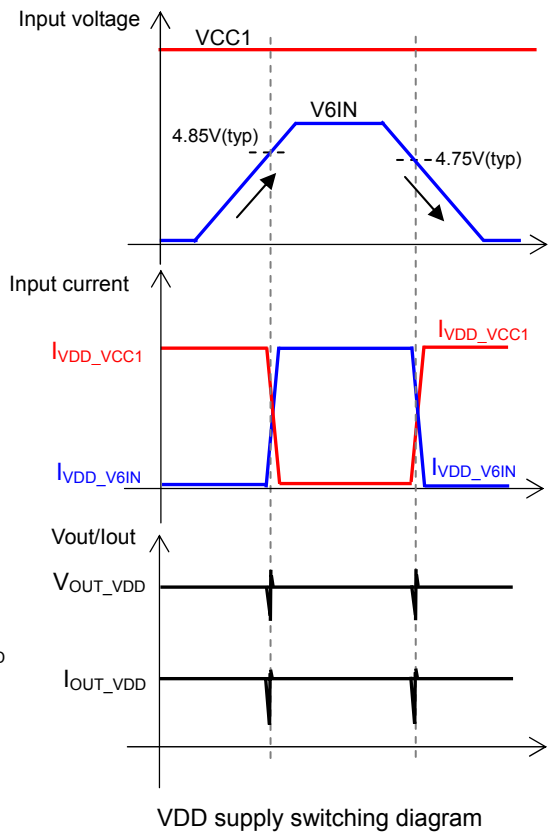
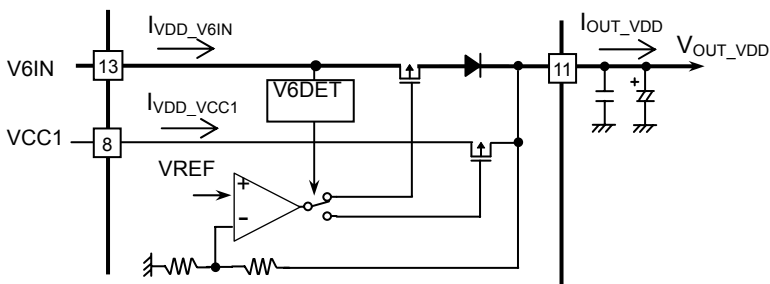
To protect the device from overheating, a thermal shutdown circuitry is included. If the junction temperature reaches approximately 175°C(typ), all outputs are turned off regardless of control state. After the junction temperature drops below 145°C(typ), VDD output is automatically restored and I²C-bus control becomes available.

The thermal shutdown circuit does not guarantee the protection of the final product because it operates out of maximum rating (exceeding T_{jmax}=150°C).

VDD regulator circuit description

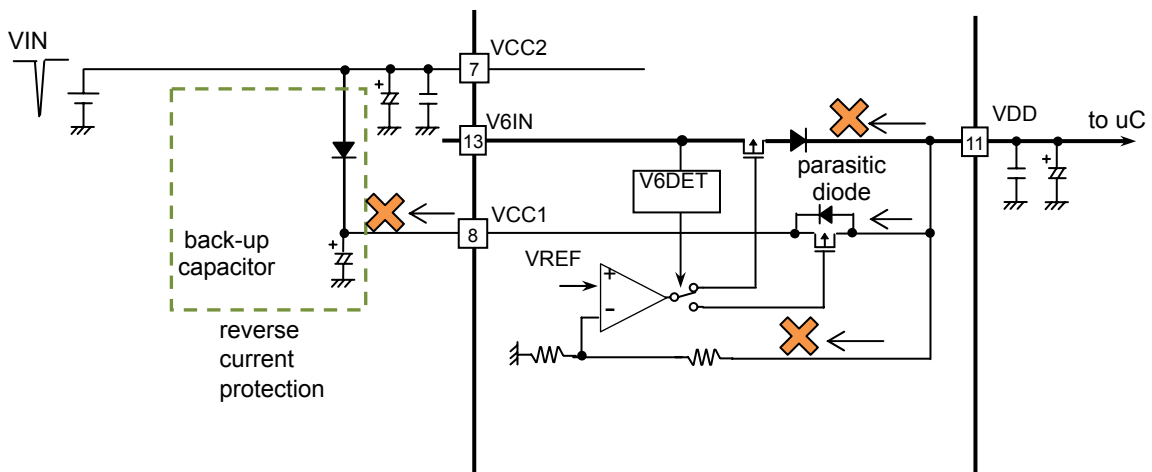
- Supply current switching

VDD output is always in operation except under thermal shut down (TSD) condition. There are 2 supply inputs (VCC1/V6IN) for this output. VCC1 is capable of high-voltage input such as car-battery. V6IN is a low voltage input and can be supplied from external DC/DC converter in order to decrease power dissipation of the device. Supply current path from VCC1 or V6IN is automatically switched depending on V6IN voltage. If V6IN voltage exceeds 4.85V(typ), V6IN supplies VDD output. Output ripple may be occurred when supply switching. This ripple can be improved by using proper output capacitor. Select appropriate capacitor suitable for your requirement.



- Reverse current protection for battery voltage black-out

There is no diode inside to prevent reverse current from VDD to VCC1. You have to add external circuit to hold VDD voltage under battery voltage black-out. There is a parasitic diode from VDD to VCC1, so insert a diode between VCC2 and VCC1 as shown figure below.



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■Pin description

| Pin # | Pin name | Function | Equivalent circuit |
|-------|----------|-------------------------------|--------------------|
| 1 | EXT | EXT output VCC2-0.5V/350mA | |
| 2 | ANT | ANT output VCC2-0.5V/300mA | |
| 3 | ILM | ILM output 5V~12V | |
| 4 | AUDIO | AUDIO output 5V~11.5V | |

Continued on next page.

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Continued from preceding page.

| Pin # | Pin name | Function | Equivalent circuit |
|-------|----------|----------------------------------|--------------------|
| 5 | CD | CD output 5V~8V/1.3A | |
| 6 | ACCIN | ACC detection input | |
| 7 | VCC2 | Supply terminal | |
| 8 | VCC1 | Supply terminal | |
| 9 | GND | GND | |
| 13 | V6IN | Supply terminal | |
| 10 | SCL | I ² C-bus clock input | |
| 11 | VDD | VDD output 3.3V/0.35A | |

Continued on next page

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Continued from preceding page.

| Pin # | Pin name | Function | Equivalent circuit |
|-------|----------|----------------------------------|--------------------|
| 12 | SDA | I ² C-bus data input | |
| 14 | FLG | FLG output | |
| 15 | SW33V | SW33V output 3.3V/5V 0.45A | |

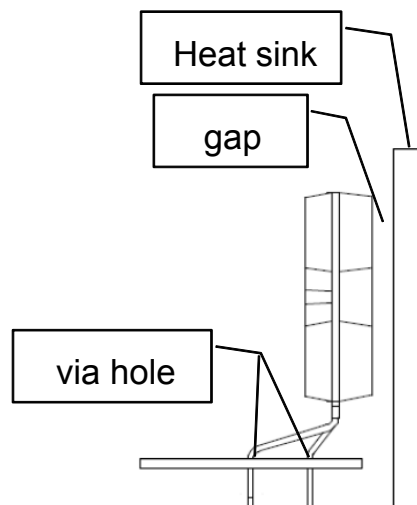
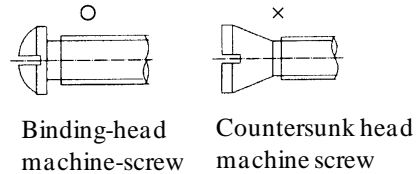
HZIP15 Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the heat generated by the device to the outer environment and dissipating that heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

b. Heat sink attachment

- Use flat-head screws to attach heat sinks.
 - Use also washer to protect the package.
 - Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
 - If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
 - **Do not make gap**, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 - **Take care a position of via hole.**
 - Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
 - Verify that there are no press burrs or screw-hole burrs on the heat sink.
 - Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
 - Twisting must be limited to under 0.05 mm.
 - **Heat sink and semiconductor device should be mounted in parallel.**
- Take care of electric or compressed air screw driver
- The speed of these torque wrenches must not exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease

- Spread the silicone grease evenly when mounting heat sinks.
- Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount

- First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,

- Take care not to allow the device to ride onto the jig or positioning dowel.
- Design the jig so that no unreasonable mechanical stress is applied to the semiconductor device.

f. Heat sink screw holes

- Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

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ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|-------------|------------------------------------|--------------------------|
| LV5685PV-XH | HZIP15 (Pb-Free / Halogen Free) | 20 / Fan-Fold |

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