1 MHz to 8 GHz, 70 dB Logarithmic Detector/Controller

Enhanced Product

AD8318-EP

FEATURES

Wide bandwidth: 1 MHz to 8 GHz
High accuracy: ±1.0 dB over 55 dB range (f < 5.8 GHz)
Stability over temperature: ±0.5 dB
Low noise measurement/controller output (VOUT)
Pulse response time: 10 ns/12 ns (fall/rise)
Integrated temperature sensor
Small footprint LFCSP
Power-down feature: <1.5 mW at 5 V
Single-supply operation: 5 V @ 68 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
RSSI measurement in base stations, WLAN, WiMAX, and radars

GENERAL DESCRIPTION

The AD8318-EP is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output voltage. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device is used in measurement or controller mode. The AD8318-EP maintains accurate log conformance for signals of 1 MHz to 6 GHz and provides useful operation to 8 GHz. The input range is typically 60 dB (re: 50 Ω) with error less than ±1 dB. The AD8318-EP has a 10 ns response time that enables RF burst detection to beyond 45 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A 2 mV/°C slope temperature sensor output is also provided for additional system monitoring. A single supply of 5 V is required. Current consumption is typically 68 mA. Power consumption decreases to <1.5 mW when the device is disabled.

The AD8318-EP can be configured to provide a control voltage to a VGA, such as a power amplifier or a measurement output, from Pin VOUT. Because the output can be used for controller applications, wideband noise is minimal.

In this mode, the setpoint control voltage is applied to VSET. The feedback loop through an RF amplifier is closed via VOUT, the output of which regulates the amplifier output to a magnitude corresponding to VSET. The AD8318-EP provides 0 V to 4.9 V output capability at the VOUT pin, suitable for controller applications. As a measurement device, Pin VOUT is externally connected to VSET to produce an output voltage, V_{OUT}, which is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is nominally −25 mV/dB but can be adjusted by scaling the feedback voltage from VOUT to the VSET interface. The intercept is 20 dBm (re: 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8318-EP is fabricated on a SiGe bipolar IC process and is available in a 4 mm × 4 mm, 16-lead LFCSP. Performance is specified over a temperature range of −55°C to +105°C.

Additional application and technical information can be found in the AD8318 data sheet.

FUNCTIONAL BLOCK DIAGRAM

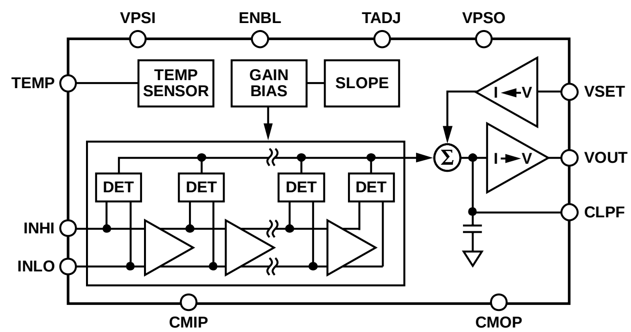

Figure 1.

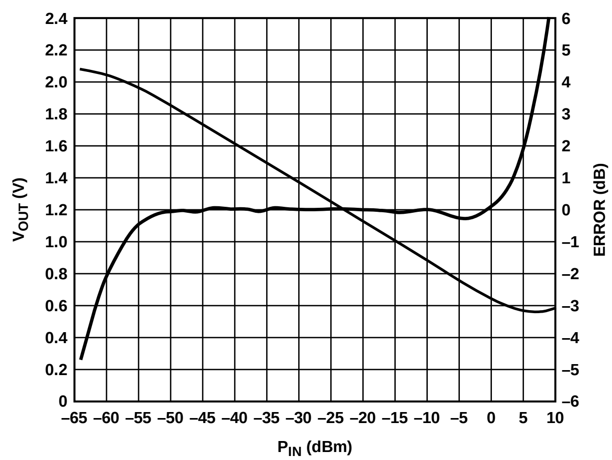

Figure 2. Typical Logarithmic Response and Error vs. Input Amplitude at 5.8 GHz

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REVISION HISTORY

7/12—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, C_{LPF} = 220 pF, T_A = 25°C, 52.3 Ω termination resistor at INHI, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHI (Pin 14) and INLO (Pin 15)				
Specified Frequency Range		0.001		8	GHz
DC Common-Mode Voltage			V_{POS} − 1.8		V
MEASUREMENT MODE	VOUT (Pin 6) shorted to VSET (Pin 7), sinusoidal input signal				
f = 900 MHz	R_{TADJ} = 500 Ω				
Input Impedance			957‖0.71		Ω‖pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
	−55°C < T_A < +105°C		63		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
Maximum Input Level	±1 dB error		−1		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope		−26	−24.5	−23	mV/dB
Intercept		19.5	22	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.7	0.78	0.86	V
Output Voltage—Low Power In	P_{IN} = −40 dBm	1.42	1.52	1.62	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.0071		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.0031		dB/°C
f = 1.9 GHz	R_{TADJ} = 500 Ω				
Input Impedance			523‖0.68		Ω‖pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
	−55°C < T_A < +105°C		63		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−59		dBm
Slope		−27	−24.4	−22	mV/dB
Intercept		17	20.4	24	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.83	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.35	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.0056		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.0004		dB/°C
f = 2.2 GHz	R_{TADJ} = 500 Ω				
Input Impedance			391‖0.66		Ω‖pF
±3 dB Dynamic Range	T_A = 25°C		65		dB
	−55°C < T_A < +105°C		62		dB
±1 dB Dynamic Range	T_A = 25°C		58		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−60		dBm
Slope		−28	−24.4	−21.5	mV/dB
Intercept		15	19.6	25	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.63	0.73	0.84	V
Output Voltage—Low Power In	P_{IN} = −35 dBm	1.2	1.34	1.5	V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.0052		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.0034		dB/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f = 3.6 GHz	R_{TADJ} = 51 Ω				
Input Impedance			119‖0.7		Ω‖pF
±3 dB Dynamic Range	T_A = 25°C		70		dB
	−55°C < T_A < +105°C		61		dB
±1 dB Dynamic Range	T_A = 25°C		58		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−60		dBm
Slope			−24.3		mV/dB
Intercept			19.8		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.717		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.46		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.0012		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.009		dB/°C
f = 5.8 GHz	R_{TADJ} = 1000 Ω				
Input Impedance			33‖0.59		Ω‖pF
±3 dB Dynamic Range	T_A = 25°C		70		dB
	−55°C < T_A < +105°C		62		dB
±1 dB Dynamic Range	T_A = 25°C		57		dB
Maximum Input Level	±1 dB error		−1		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			−24.3		mV/dB
Intercept			25		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		0.86		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.59		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.019		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.0096		dB/°C
f = 8.0 GHz	R_{TADJ} = 500 Ω				
±3 dB Dynamic Range	T_A = 25°C		60		dB
	−55°C < T_A < +105°C		58		dB
Maximum Input Level	±3 dB error		3		dBm
Minimum Input Level	±3 dB error		−55		dBm
Slope			−23		mV/dB
Intercept			37		dBm
Output Voltage—High Power In	P_{IN} = −10 dBm		1.06		V
Output Voltage—Low Power In	P_{IN} = −40 dBm		1.78		V
Temperature Sensitivity	P_{IN} = −10 dBm				
	25°C ≤ T_A ≤ 105°C		0.032		dB/°C
	−55°C ≤ T_A ≤ +25°C		0.0078		dB/°C
OUTPUT INTERFACE	VOUT (Pin 6)				
Voltage Swing	V_{SET} = 0 V; P_{IN} = −10 dBm, no load[1]		4.9		V
	V_{SET} = 2.1 V; P_{IN} = −10 dBm, no load[1]		25		mV
Output Current Drive	V_{SET} = 1.5 V; P_{IN} = −50 dBm		60		mA
Small Signal Bandwidth	P_{IN} = −10 dBm; from CLPF to VOUT		60		MHz
Video Bandwidth (or Envelope Bandwidth)			45		MHz
Output Noise	P_{IN} = 2.2 GHz; −10 dBm, f_{NOISE} = 100 kHz, C_{LPF} = 220 pF		90		nV/√Hz
Fall Time	P_{IN} = Off to −10 dBm, 90% to 10%		10		ns
Rise Time	P_{IN} = −10 dBm to off, 10% to 90%		12		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VSET INTERFACE	VSET (Pin 7)				
Nominal Input Range	P_{IN} = 0 dBm; measurement mode[2]		0.5		
	P_{IN} = −65 dBm; measurement mode[2]		2.1		V
Logarithmic Scale Factor			−0.04		dB/mV
Bias Current Source	P_{IN} = −10 dBm; V_{SET} = 2.1 V		2.5		μA
TEMPERATURE REFERENCE	TEMP (Pin 13)				
Output Voltage	T_A = 25°C, R_{LOAD} = 10 kΩ	0.57	0.6	0.63	V
Temperature Slope	−55°C ≤ T_A ≤ +105°C, R_{LOAD} = 10 kΩ		2		mV/°C
Current Source/Sink	T_A = 25°C		10/0.1		mA
POWER-DOWN INTERFACE	ENBL (Pin 16)				
Logic Level to Enable Device			1.7		V
ENBL Current When Enabled	ENBL = 5 V		<1		μA
ENBL Current When Disabled	ENBL = 0 V; sourcing		15		μA
POWER INTERFACE	VPSI (Pin 3 and Pin 4), VPSO (Pin 9)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	ENBL = 5 V	50	68	82	mA
vs. Temperature	−55°C ≤ T_A ≤ +105°C		150		μA/°C
Supply Current when Disabled	ENBL = 0 V, total currents for VPSI and VPSO		260		μA
vs. Temperature	−55°C ≤ T_A ≤ +105°C		350		μA

[1] Controller mode.
[2] Gain = 1. For other gains, see the AD8318 data sheet.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: Pin VPSO, Pin VPSI	5.7 V
ENBL, V_{SET} Voltage	0 to V_{POS}
Input Power (Single-Ended, re: 50 Ω)	12 dBm
Internal Power Dissipation	0.73 W
$θ_{JA}$[1]	55°C/W
Maximum Junction Temperature	130°C
Operating Temperature Range	−55°C to +105°C
Storage Temperature Range	−65°C to +150°C

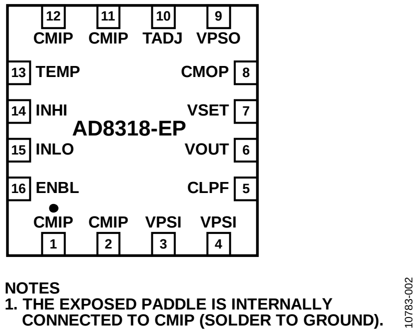
[1] With package die paddle soldered to thermal pads with vias connecting to inner and bottom layers.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE IS INTERNALLY CONNECTED TO CMIP (SOLDER TO GROUND).

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 11, 12	CMIP	Device Common (Input System Ground).
3, 4	VPSI	Positive Supply Voltage (Input System): 4.5 V to 5.5 V. Voltage on Pin 3, Pin 4, and Pin 9 should be equal.
5	CLPF	Loop Filter Capacitor.
6	VOUT	Measurement and Controller Output.
7	VSET	Setpoint Input for Controller Mode or Feedback Input for Measurement Mode.
8	CMOP	Device Common (Output System Ground).
9	VPSO	Positive Supply Voltage (Output System): 4.5 V to 5.5 V. Voltage on Pin 3, Pin 4, and Pin 9 should be equal.
10	TADJ	Temperature Compensation Adjustment.
13	TEMP	Temperature Sensor Output.
14	INHI	RF Input. Nominal input range: –60 dBm to 0 dBm (re: 50 Ω), ac-coupled.
15	INLO	RF Common for INHI. AC-coupled RF common.
16	ENBL	Device Enable. Connect to VPSI for normal operation. Connect pin to ground for disable mode.
	Paddle	The Exposed Paddle is Internally Connected to CMIP (Solder to Ground).

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V; T_A = +25°C, −55°C, +105°C; C_{LPF} = 220 pF; R_{TADJ} = 500 Ω; unless otherwise noted. Colors: +25°C → Black; −55°C → Blue; +105°C → Red.

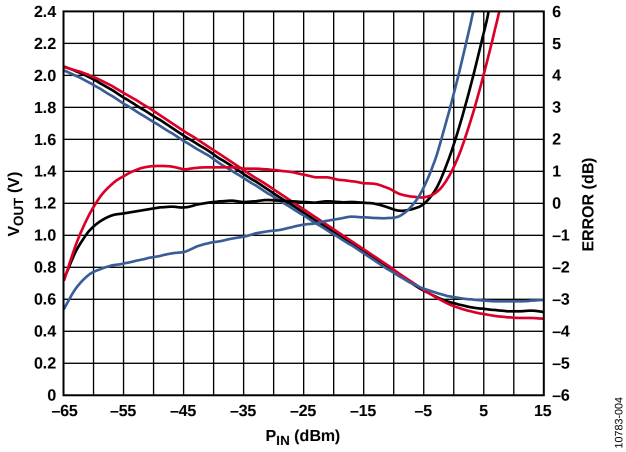


Figure 4. VOUT and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device

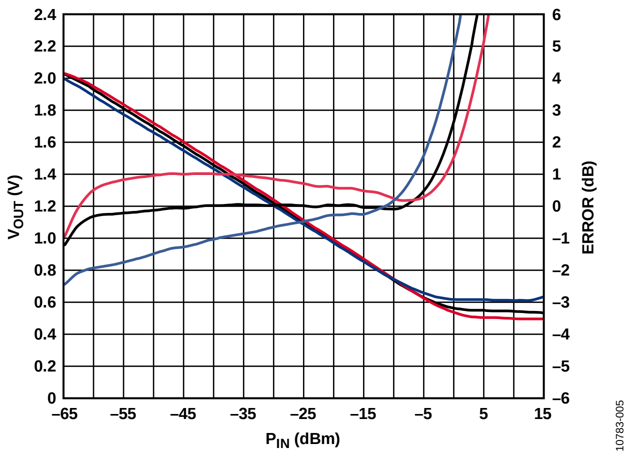


Figure 5. VOUT and Log Conformance vs. Input Amplitude at 1.9 GHz, Typical Device

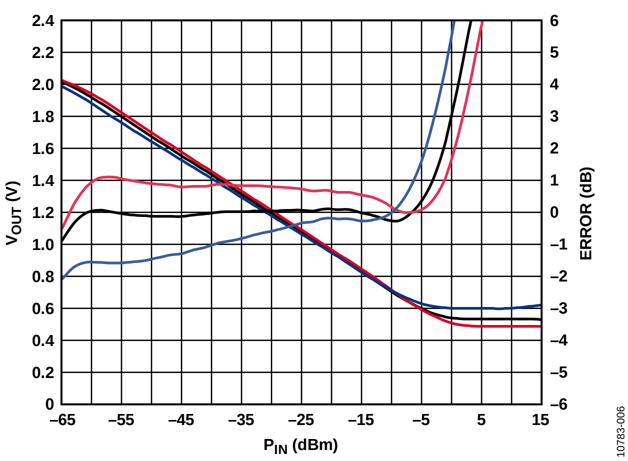


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, Typical Device

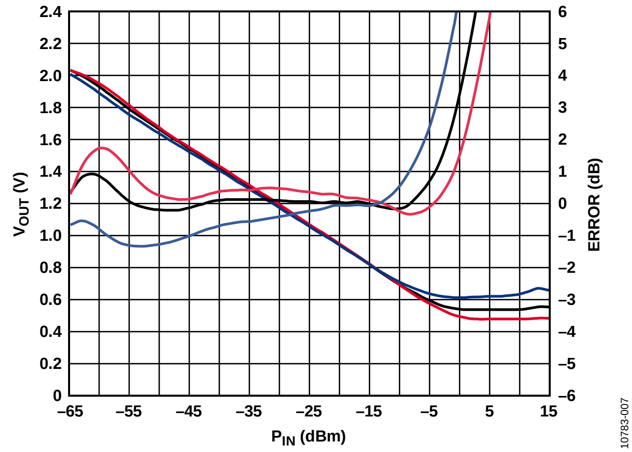


Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, Typical Device, R_{TADJ} = 51 Ω

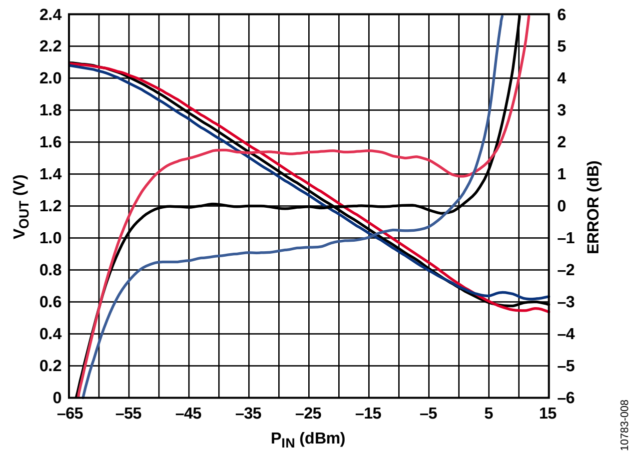


Figure 8. VOUT and Log Conformance vs. Input Amplitude at 5.8 GHz, Typical Device, R_{TADJ} = 1000 Ω

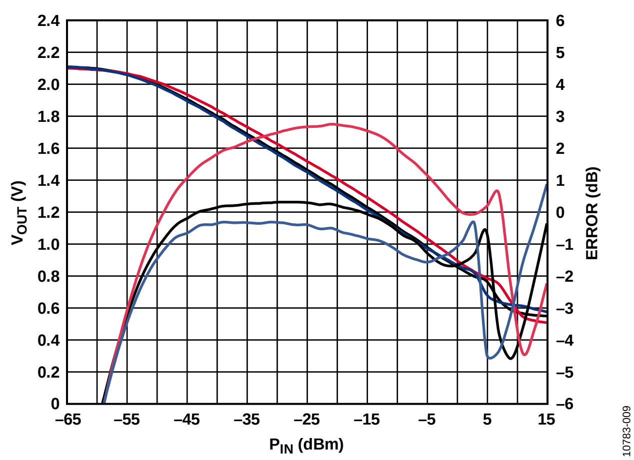


Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 8 GHz, Typical Device

V_{POS} = 5 V; T_A = +25°C, −55°C, +105°C; C_{LPF} = 220 pF; R_{TADJ} = 500 Ω; unless otherwise noted. Colors: +25°C → Black; −55°C → Blue; +105°C → Red.

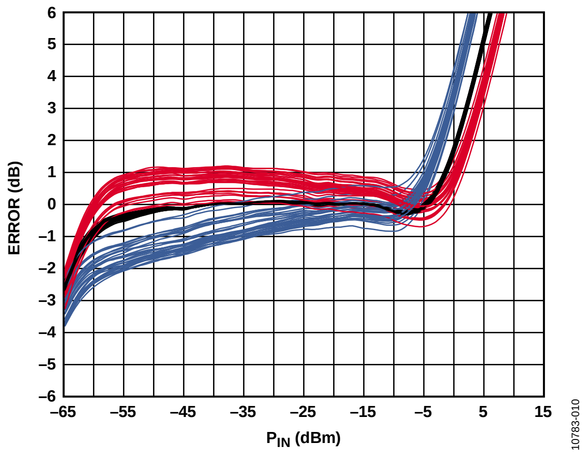


Figure 10. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude at 900 MHz for at Least 70 Devices

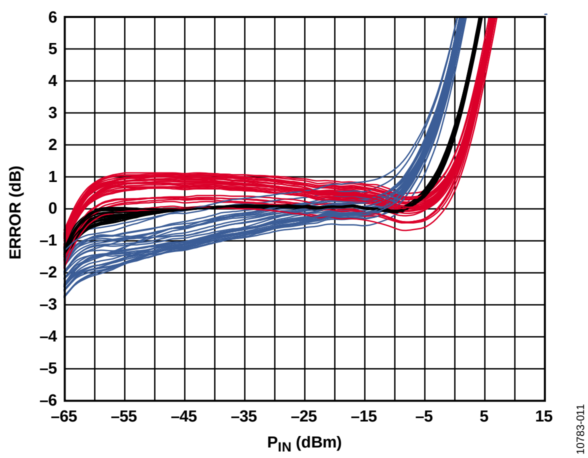


Figure 11. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 1900 MHz for at Least 70 Devices

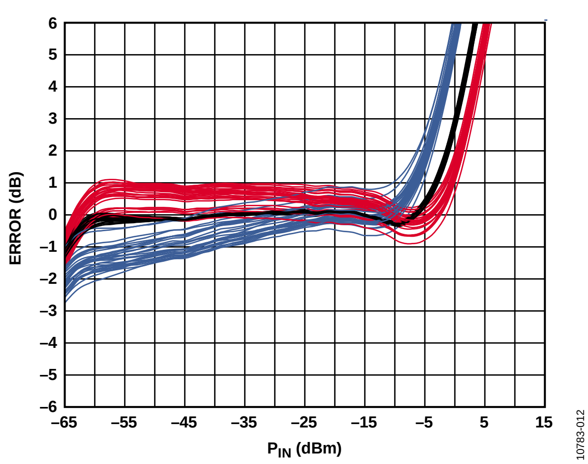


Figure 12. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 2.2 GHz for at Least 70 Devices

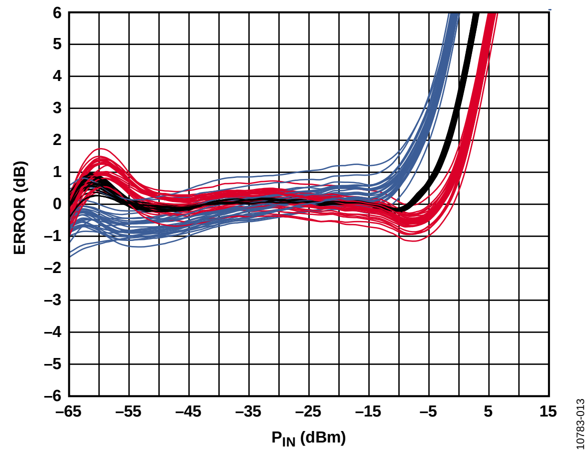


Figure 13. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 3.6 GHz for at Least 70 Devices, R_{TADJ} = 51 Ω

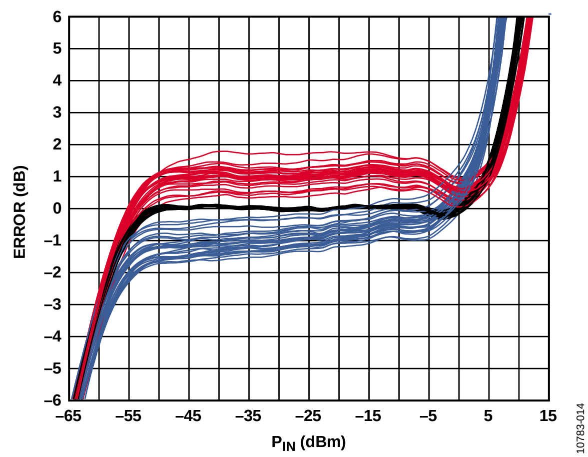


Figure 14. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 5.8 GHz for at Least 70 Devices, R_{TADJ} = 1000 Ω

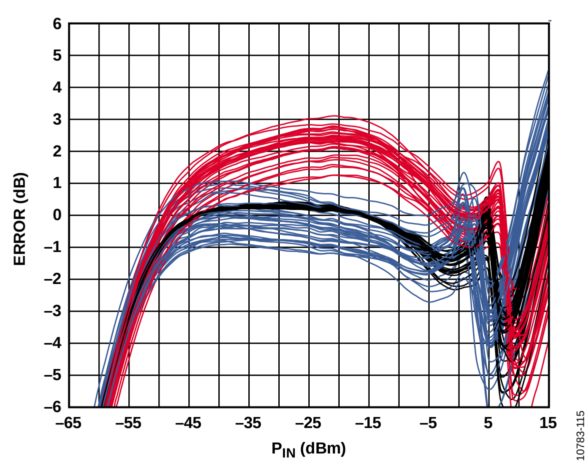


Figure 15. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude at 8 GHz for at Least 70 Devices

V_{POS} = 5 V; T_A = +25°C, −55°C, +105°C; C_{LPF} = 220 pF; R_{TADJ} = 500 Ω; unless otherwise noted. Colors: +25°C → Black; −55°C → Blue; +105°C → Red.

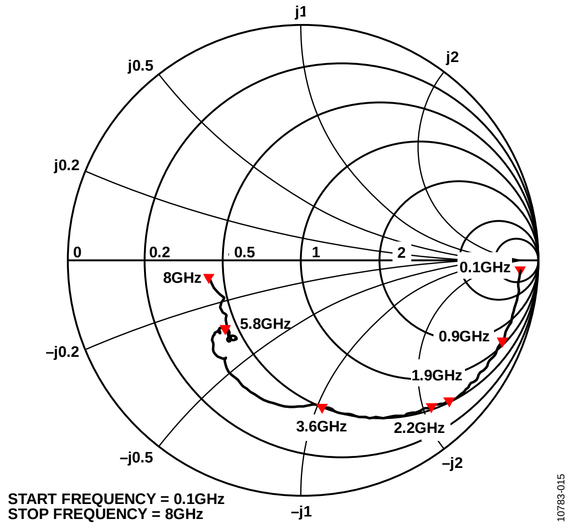


Figure 16. Input Impedance vs. Frequency; No Termination Resistor on INHI, Z_O = 50 Ω

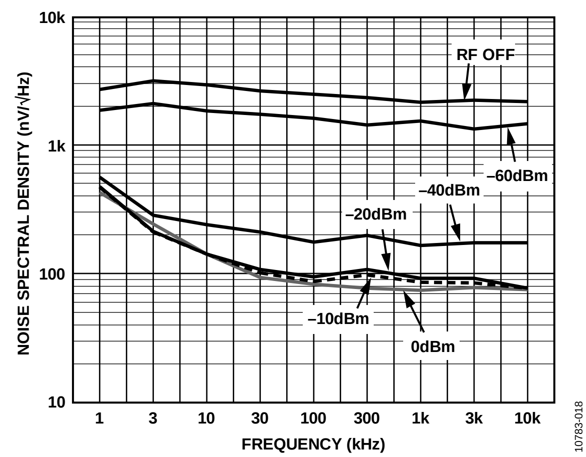


Figure 19. Noise Spectral Density of Output; CLPF = Open

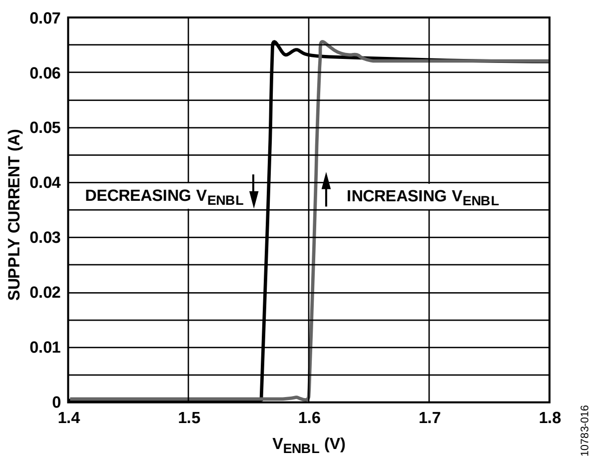


Figure 17. Supply Current vs. Enable Voltage

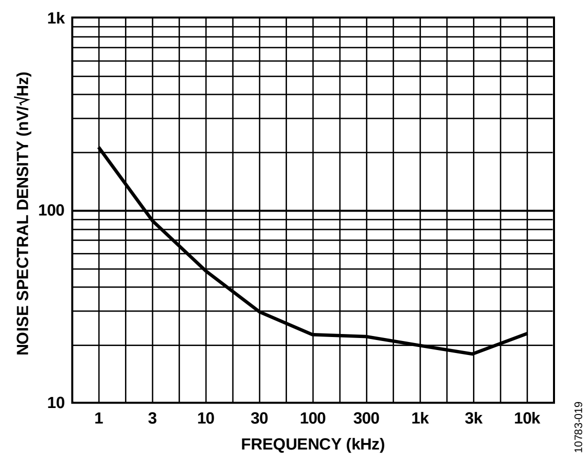


Figure 20. Noise Spectral Density of Output Buffer (from CLPF to VOUT); CLPF = 0.1 μF

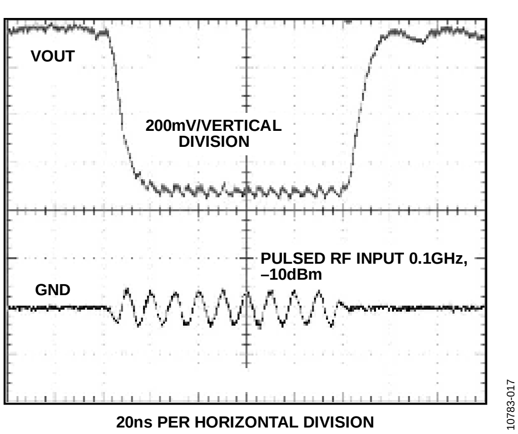


Figure 18. VOUT Pulse Response Time; Pulsed RF Input 0.1 GHz, −10 dBm; CLPF = Open

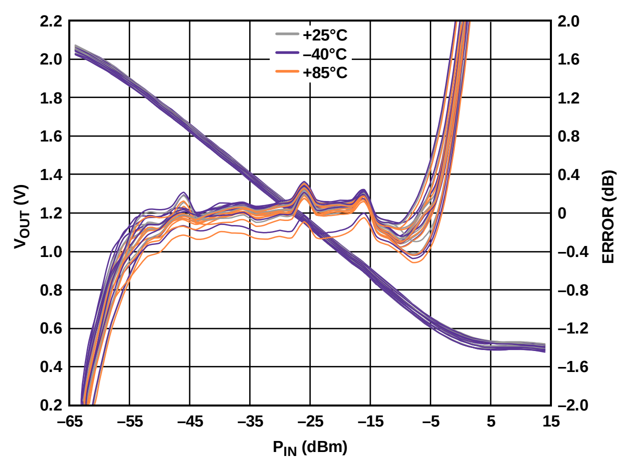


Figure 21. Output Voltage Stability vs. Supply Voltage at 1.9 GHz When VP Varies by 10%, Multiple Devices

OUTLINE DIMENSIONS

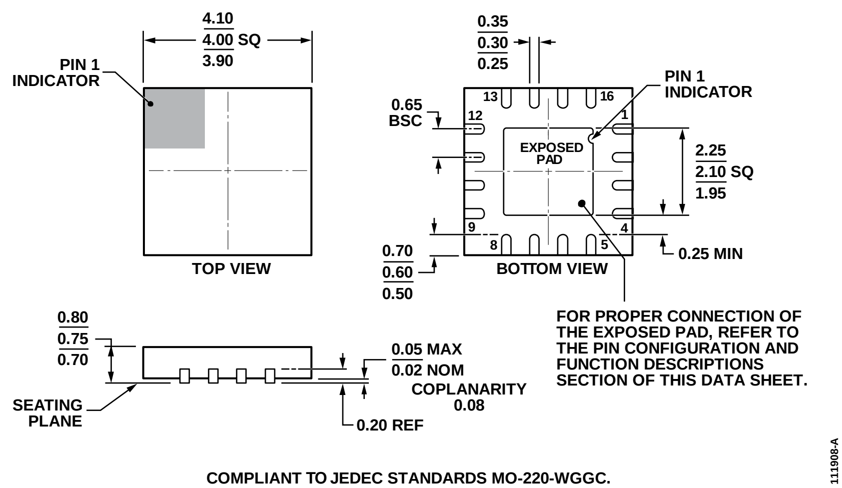


Figure 22. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8318SCPZ-EP-RL7	−55°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	1,500
AD8318SCPZ-EP-R2	−55°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	250
AD8318SCPZ-EP-WP	−55°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	64
AD8318-EP-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] WP = waffle pack.

NOTES