

## PIC18F2515/2610/4515/4610 Rev. A3 Silicon Errata

The PIC18F2515/2610/4515/4610 Rev. A3 parts you have received conform functionally to the Device Data Sheet (DS39636D), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2515/2610/4515/4610 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

**The following silicon errata apply only to PIC18F2515/2610/4515/4610 devices with these Device/Revision IDs:**

Part Number	Device ID	Revision ID
PIC18F2515	0000 1100 111	0 0011
PIC18F2610	0000 1100 101	0 0011
PIC18F4515	0000 1100 011	0 0011
PIC18F4610	0000 1100 001	0 0011

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

### 1. Module: MSSP

In its current implementation, the I<sup>2</sup>C™ Master mode operates as follows:

- a) The Baud Rate Generator for I<sup>2</sup>C in Master mode is slower than the rates specified in Table 16-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 16-3 of the Device Data Sheet. The differences are shown in **bold** text.

- b) Use the following formula in place of the one shown in Register 16-4 (SSPCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = 1000.

$$SSPADD = \text{INT}((F_{CY}/F_{SCL}) - (F_{CY}/1.111 \text{ MHz})) - 1$$

**Date Codes that pertain to this issue:**

All engineering and production devices.

**TABLE 1: I<sup>2</sup>C™ CLOCK RATE w/BRG**

Fosc	Fcy	Fcy * 2	BRG Value	Fscl (2 Rollovers of BRG)
<b>40 MHz</b>	10 MHz	20 MHz	<b>0Eh</b>	400 kHz <sup>(1)</sup>
<b>40 MHz</b>	10 MHz	20 MHz	<b>15h</b>	312.5 kHz
<b>40 MHz</b>	10 MHz	20 MHz	<b>59h</b>	100 kHz
<b>16 MHz</b>	4 MHz	8 MHz	<b>05h</b>	400 kHz <sup>(1)</sup>
<b>16 MHz</b>	4 MHz	8 MHz	<b>08h</b>	308 kHz
<b>16 MHz</b>	4 MHz	8 MHz	<b>23h</b>	100 kHz
<b>4 MHz</b>	1 MHz	2 MHz	<b>01h</b>	333 kHz <sup>(1)</sup>
<b>4 MHz</b>	1 MHz	2 MHz	<b>08h</b>	100 kHz
<b>4 MHz</b>	1 MHz	2 MHz	00h	1 MHz <sup>(1)</sup>

**Note 1:** The I<sup>2</sup>C™ interface does not conform to the 400 kHz I<sup>2</sup>C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

# PIC18F2515/2610/4515/4610

## 2. Module: MSSP

When the MSSP is configured for SPI Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

### Work around

Use Rev. A4 silicon devices.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 3. Module: MSSP

After an I<sup>2</sup>C transfer is initiated, the SSPBUF register may be written for up to 10 T<sub>cy</sub> before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

### Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 4. Module: MSSP

In 10-Bit Addressing mode, when a Repeated Start is issued followed by the high address byte and a write command (R/W = 0), an ACK is not issued.

### Work around

There are two work arounds available:

#### 1. Single Master Environment:

In a single master environment, the user must issue a Stop, then a Start followed by a write to the address high, then the address low followed by the data.

#### 2. Multi-Master Environment:

In a multi-master environment, the user must issue a Repeated Start, send a dummy write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will help maintain control of the bus.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 5. Module: ECCP

When the ECCP1 auto-shutdown feature is configured for automatic restart by setting the PRSEN bit (PWM1CON<7>), the pulse terminates immediately in a shutdown event. In addition, the pulse may restart within the period if the shutdown condition expires. This may result in the generation of short pulses on the PWM output(s).

### Work around

Configure the auto-shutdown for software restart by clearing the PRSEN bit (PWM1CON<7>). The PWM can be re-enabled by clearing the ECCPASE bit (ECCP1AS<7>) after the shutdown condition expires.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 6. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

### Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 1, ECCPASE bit operations are performed on the W register.

### EXAMPLE 1: BIT OPERATIONS IN WORKING REGISTER

```
MOVWF ECCP1AS, W
BTFSC WREG, ECCPASE
BRA SHUTDOWN_ROUTINE
```

### Date Codes that pertain to this issue:

All engineering and production devices.

## 7. Module: ECCP

The auto-shutdown source, FLT0, has inverse polarity from the description in **Section 15.4.7 “Enhanced PWM Auto-Shutdown”** of the Device Data Sheet. A logic high-voltage level on FLT0 will generate a shutdown on ECCP1.

### Work around

None.

### Date Codes that pertain to this issue:

All engineering and production devices.

# PIC18F2515/2610/4515/4610

## 8. Module: ECCP and CCP

The ECCP1 and CCP2 configured for PWM mode, with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

### Work around

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The ECCP and CCP modules remain capable of 10-bit accuracy.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 9. Module: A/D

The A/D offset is greater than the specified limit in Table 25-24 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 2.

### Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

### Date Codes that pertain to this issue:

All engineering and production devices.

**TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18F2X1X/4X1X (INDUSTRIAL, EXTENDED) PIC18LF2X1X/4X1X (INDUSTRIAL)**

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
A06A	E0FF	<b>Offset Error</b>	—	—	<b>&lt;±2.0</b>	LSb	<b>VREF = VREF+ and VREF-</b>
A06	E0FF	Offset Error	—	—	<b>&lt;±3.5</b>	LSb	<b>VREF = Vss and VDD</b>

## 10. Module: BOR

The BOR module may reset below the minimum operating voltage of the device when configured for BORV1:BORV0 = 11. The updated Reset voltage specifications are shown in **bold** in Table 3.

**TABLE 3: BROWN-OUT RESET VOLTAGE**

Param No.	Sym.	Characteristic	Min.	Typ.	Max.	Unit
D005	VBOR	<b>Brown-out Reset Voltage</b>				
		PIC18LF2515/2610/4515/4610				
		BORV1:BORV0 = 11	<b>N/A</b>	2.05	<b>N/A</b>	V

### Work around

Use the next higher BOR voltage setting to ensure a low VDD is detected above 2.0V.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 11. Module: ECCP

ECCP1 configured for auto-shutdown with Comparator 1 corrupts the PWM duty cycle pulse. In addition, it does not always synchronize the pulse to the beginning of the period and the end of the pulse can occur at any time within the period.

### Work around

Use FLT0 for the auto-shutdown source. Applications which can tolerate a shutdown response time of several TCYS may use the comparator interrupt flag to detect a shutdown event and disable the PWM by clearing the EECPPASE bit (ECCP1AS<7>).

### Date Codes that pertain to this issue:

All engineering and production devices.

# PIC18F2515/2610/4515/4610

---

## 12. Module: ECCP

When the shutdown state of the PWM pin(s) is configured to tri-state the outputs, the device may consume higher than expected current during the shutdown event.

### Work around

Configure the PWM output for either a high or low logic state during the shutdown via the PSSAC1:PSSAC0 (ECCP1AS<3:2>) and PSSBD1: PSSBD0 (ECCP1AS<1:0>) bits. Clearing the auto-shutdown event will return the device to normal current consumption levels.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 13. Module: ECCP

The PWM pin(s) may change state if a breakpoint is encountered during emulation and an auto-shutdown event occurs via FLT0. This affects the MPLAB® ICD 2 debugger and the ICE 2000 and ICE 4000 emulators.

### Work around

During emulation, use the comparator for auto-shutdown. Applications which can tolerate a shutdown response time of several Tcys may use the external interrupt flag, INT0IF, to detect a shutdown event and disable the PWM by clearing the ECCPASE bit (ECCP1AS<7>).

### Date Codes that pertain to this issue:

All engineering and production devices.

## 14. Module: ECCP and CCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP/CCP in Compare mode with the Special Event Trigger (CCP1CON bits, CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next prescaler output pulse after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

### Work around

To achieve the same timer Reset period on the PIC18F4610 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F4610 family, use CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 15. Module: ECCP

When a shutdown condition occurs, the output port(s) is made inactive for the duration of the event. After the event that caused the shutdown ends, the ECCP module enables the PWM output right away instead of waiting until the beginning of the next PWM cycle.

### Work around

Disable the auto-restart feature in software, polling the Timer2 Interrupt Flag, TMR2IF, and wait until it is set before clearing the ECCPASE bit.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 16. Module: ECCP

When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.

### Work around

Disable the PWM or set duty cycle to zero prior to switching directions.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 17. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the baud rate timer which will effect any ongoing transmission.

### Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

### Date Codes that pertain to this issue:

All engineering and production devices.

## 18. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), the second byte may be corrupted if it is written into TXREG immediately after the TMRT bit is set.

### Work around

Execute a software delay, at least one half the transmission's bit time, after TMRT is set and prior to writing subsequent bytes into TXREG.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 19. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for the external clock source and the CCPxCON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

### Work around

Modify firmware to reset the Timer registers upon detection of the compare match condition — TMRxL and TMRxH.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 20. Module: Timer1/Timer3

When Timer1 or Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 T<sub>cy</sub>, interrupts will occasionally be skipped.

### Work around

Avoid using an external clock with a period (1/frequency) between 1 and 2 T<sub>cy</sub>.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 21. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H were written.

### Work around

Two work arounds are available: 1) Stop Timer1/Timer3 before writing the TMR1H/TMR3H registers; 2) Write TMR1L/TMR3L immediately after writing TMR1H/TMR3H.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 22. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

### Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.

# PIC18F2515/2610/4515/4610

---

- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 2.

## EXAMPLE 2: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;           //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                   //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2Tcy before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                                //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                          //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

## 23. Module: MSSP

I<sup>2</sup>C Receive mode should be enabled (i.e., RCEN bit should be set) only when the system is idle (i.e., when ACKEN, RCEN, PEN, RSEN and SEN all equal zero). It should not be possible to set the RCEN bit when the system is not idle, however, the RCEN bit can be set under this circumstance.

### Work around

Wait for the system to become idle before setting the RCEN bit. This requires a check for the following bits to be clear:

ACKEN, RCEN, PEN, RSEN and SEN.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 24. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of TEMP before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`  
where Fd is WREG, BSR or STATUS;

`MOVSF Zs, Fd`  
where Fd is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`  
where the destination is WREG, BSR or STATUS.

## Work around

1. Assembly Language Programming:

- a) If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 8-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

```
MOVF    TEMP, W
MOVWF   BSR
```

instead of `MOVFF TEMP, BSR`.

- b) As another alternative, the following work around shown in Example 3 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

### EXAMPLE 3: DUMMY CALL ROUTINE

```
ISR @ 0x0008
CALL    Foo, FAST      ; store current value of WREG, BSR, STATUS for a second time
Foo:
POP     ; clears return address of Foo call
:      ; insert high priority ISR code here
:
RETFIE  FAST
```

# PIC18F2515/2610/4515/4610

---

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

The code segment shown in Example 4 demonstrates the work around using the C18 compiler:

**Date Codes that pertain to this issue:**

All engineering and production devices.

## EXAMPLE 4: C18 COMPILER EXAMPLE

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```



# PIC18F2515/2610/4515/4610

---

An optimized C18 version is also provided in Example 5. This example illustrates how it reduces the instruction cycle count from 10 cycles to 3:

## EXAMPLE 5: OPTIMIZED C18 COMPILER EXAMPLE

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
    _asm
        CALL high_vector_branch, 1
    _endasm
}

void high_vector_branch (void)
{
    _asm
        POP
        GOTO high_isr
    _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
    ...
}
```

# PIC18F2515/2610/4515/4610

---

## 25. Module: EUSART

The EUSART auto-baud feature may occasionally measure the incoming baud rate incorrectly. The rate of incorrect baud rate measurements will depend on the frequency of the incoming synchronization byte and the system clock frequency.

### Work around

None.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 26. Module: EUSART

In Synchronous mode (SYNC = 1) with clock polarity high (SCKP = 1), the EUSART transmits a shorter than expected clock on the CK pin for bit 0.

### Work around

None.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 27. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.

### Work around

Use another baud rate configuration to generate the desired baud rate.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 28. Module: EUSART

During an auto-baud operation, the TX pin is tri-stated. Transceivers which do not provide a pull-up on the TX signal may cause the bus to become inadvertently active and prevent additional bus activity.

### Work around

Use pull-up resistor on TX pin.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 29. Module: MSSP

In an I<sup>2</sup>C system with multiple slave nodes, an unaddressed slave may respond to bus activity when data on the bus matches its address. The first occurrence will set the BF bit. The second occurrence will set the BF and the SSPOV bits. In both situations, the SSPIF bit is not set and an interrupt will not occur.

### Work around

The I<sup>2</sup>C slave must clear the SSPOV bit after each I<sup>2</sup>C event to maintain normal operation.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 30. Module: MSSP

In I<sup>2</sup>C Master mode, the BRG value of '0' may not work correctly.

### Work around

Use a BRG value greater than '0' by setting SSPADD ≥ '1'.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 31. Module: MSSP

In I<sup>2</sup>C Master mode, the RCEN bit is set by software to begin data reception and cleared by the peripheral after a byte is received. After a byte is received, the device may delay clearing RCEN.

### Work around

Single byte receptions are typically not affected, since the delay between byte receptions typically is long enough for the RCEN bit to clear. For multiple byte receptions, the software must wait until the bit is cleared before the next byte can be received.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 32. Module: MSSP

Setting the SEN bit initiates a Start sequence on the bus, after which, the SEN bit is cleared automatically by hardware. If the SEN bit is set again (without an address byte being transmitted), a Start sequence will not commence and the SEN bit will not be cleared. This condition causes the bus to remain in an active state. The system is Idle when ACKEN, RCEN, PEN, RSEN, and SEN are clear.

### Work around

Set the PEN or RSEN bit to transmit a Stop or Repeated Start sequence, although the SEN bit may still be set, indicating the bus is active. After the sequence has completed, the PEN, RSEN and SEN bit will be clear, indicating the bus is Idle. Clearing and setting the SSPEN bit will also reset the I<sup>2</sup>C peripheral and clear the PEN, RSEN and SEN status bits.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 33. Module: MSSP

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL bit in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

### Work around

Ensure that if the buffer is full, SSPBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

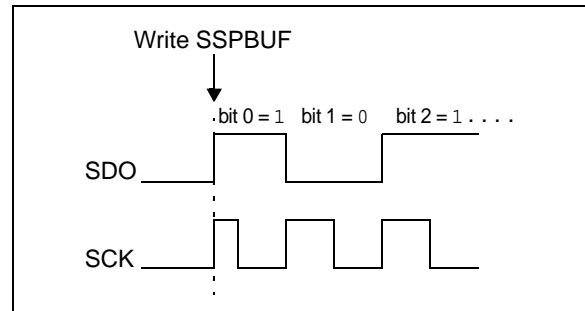
### Date Codes that pertain to this issue:

All engineering and production devices.

## 34. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

**FIGURE 1: SCK PULSE VARIATION USING TIMER2/2**



### Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 6 for sample code.

**EXAMPLE 6: AVOIDING THE INITIAL SHORT SCK PULSE**

```

LOOP BTFSS SSPSTAT, BF      ;Data received?
                                ;(Xmit complete?)
    BRA LOOP                ;No
    MOVF SSPBUF, W          ;W = SSPBUF
    MOVWF RXDATA            ;Save in user RAM
    MOVF TXDATA, W         ;W = TXDATA
    BCF T2CON, TMR2ON      ;Timer2 off
    CLRF TMR2              ;Clear Timer2
    MOVWF SSPBUF           ;Xmit New data
    BSF T2CON, TMR2ON      ;Timer2 on
    
```

### Date Codes that pertain to this issue:

All engineering and production devices.

# PIC18F2515/2610/4515/4610

## 35. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREG, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to;
- The baud rate counter overflows (at the end of the bit period); and
- A Stop bit is being transmitted (shifted out of TSR).

### Work around

If possible, do not use the module's double buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREG immediately after TXIF is set or wait 1-bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted. Note that TXIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREG
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of Stop bit, then start the timer when you load the TXREG. Do not load the TXREG when timer is about to overflow.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 36. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, the received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after the RCIDL bit (BAUDCON<6>) is set.

### Work around

Write to TX9D only when a reception is not in progress (RCIDL = 1). Since there is no interrupt associated with RCIDL, it must be polled in software to determine when TX9D can be updated.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 37. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREG, the value is no longer valid for subsequent read operations.

### Work around

The RCREG register should only be read once for each byte received. After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL bit (BAUDCON<6>) for a low-to-high transition, or use the EUSART receive interrupt, RCIF (PIR1<5>).

### Date Codes that pertain to this issue:

All engineering and production devices.

## 38. Module: EUSART

With the auto-wake-up option enabled by setting the WUE (BAUDCON<1>) bit, the RCIF (PIR1<5>) bit will become set on a high-to-low transition on the RX pin. However, the WUE bit may not clear within 1 T<sub>cy</sub> of a low-to-high transition on RX. While the WUE bit is set, reading the receive buffer, RCREG, will not clear the RCIF interrupt flag. Therefore, the first opportunity to automatically clear RCIF by reading RCREG may take longer than expected.

<b>Note:</b> RCIF can only be cleared by reading RCREG.
---

### Work around

There are two work arounds available:

1. Clear the WUE bit in software after the wake-up event has occurred prior to reading the receive buffer, RCREG.
2. Poll the WUE bit and read RCREG after the WUE bit is automatically cleared.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 39. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increments and set the interrupt flags as expected. The timer registers can also be written as expected.

### **Work around**

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the T1SYNC bit (T1CON<2>).

### **Date Codes that pertain to this issue:**

All engineering and production devices.

## 40. Module: MSSP

The MSSP configured in SPI Slave mode will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP by clearing and setting the SSPEN (SSPCON1<5>) bit prior to rewriting SSPBUF will not prevent the error condition.

### **Work around**

Prior to updating the SSPBUF register with a new value, verify whether the previous contents were transferred by reading the BF (SSPSTAT<0>) bit. If the previous byte has not been transferred, update SSPBUF and clear the WCOL (SSPCON1<7>) bit if necessary.

### **Date Codes that pertain to this issue:**

All engineering and production devices.

## 41. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

### **Work around**

None

### **Date Codes that pertain to this issue:**

All engineering and production devices.

## 42. Module: MSSP

It has been observed that following a Power-on Reset, I<sup>2</sup>C mode may not initialize properly by just configuring the SCL and SDA pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

### **Work around**

Before configuring the module for I<sup>2</sup>C operation:

1. Configure the SCL and SDA pins as outputs by clearing their corresponding TRIS bits.
2. Force SCL and SDA low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCL and SDA as inputs by setting their TRIS bits.

Once this is done, use the SSPCON1 and SSPCON2 registers to configure the proper I<sup>2</sup>C mode as before.

### **Date Codes that pertain to this issue:**

All engineering and production devices.

# PIC18F2515/2610/4515/4610

---

## 43. Module: MSSP

When the MSSP is configured for SPI mode, the Buffer Full Status bit, BF (SSPSTAT<0>), should not be polled in software to determine when the transfer is complete.

### Work around

Copy the SSPSTAT register into a variable and perform the bit test on the variable. In Example 7, SSPSTAT is copied into the working register where the bit test is performed.

### EXAMPLE 7: BIT TEST EXAMPLE

```
loop_MSB:
    MOVF    SSPSTAT, W
    BTFSS  WREG, BF
    BRA     loop_MSB
```

A second option is to poll the Master Synchronous Serial Port Interrupt Flag bit, SSPIF (PIR1<3>). This bit can be polled and will set when the transfer is complete.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 44. Module: Reset

This version of silicon does not support the functionality described in Note 1 of parameter D002 in **Section 25.1 “DC Characteristics: Supply Voltage”** of the data sheet. The RAM content may be altered during a Reset event if following conditions are met.

- Device is accessing RAM.
- Asynchronous Reset (i.e., WDT, BOR or  $\overline{\text{MCLR}}$ ) occurs when a write operation is being executed (start of a Q4 cycle).

### Work around

None

### Date Codes that pertain to this issue:

All engineering and production devices.

## 45. Module: 10-Bit Analog-to-Digital (A/D) Converter Module

When the A/D clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EdL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

### Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC, 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

### Date Codes that pertain to this issue:

All engineering and production devices.

## REVISION HISTORY

### Rev A Document (8/2004)

First revision of this document.

Issues 1-4 (MSSP), 5-7 (ECCP), 8 (ECCP and CCP), 9 A/D, and 10 (DC Characteristics). Data Sheet Clarification issues 1 (I/O Ports) and 2 (Resets).

### Rev B Document (2/2005)

Added Date Code information to all issues, updated text and reordered issues for clarity.

Issues in this revision are: 1-4, 22 (MSSP), 5-7, 11-13, 15-16 (ECCP), 8, 14 (ECCP and CCP), 9 (A/D), 10 (BOR), 17-18 (EUSART), 19-21 (Timer1/Timer3) and 23 (Interrupts).

### Rev C Document (9/2005)

Updated issue 4 (MSSP), issue 8 (ECCP and CCP) and issue 23 (Interrupts), and added issues 24-27 (EUSART), 28-32 (MSSP), 33 (SSP – SPI mode) and 34 (Timer1 – Asynchronous Counter).

### Rev D Document (4/2006)

Removed previous issue 34 (Timer1 – Asynchronous Counter). Added Example 4 in issue 23 (Interrupts). Added issues 34-37 (EUSART), 38 (Timer1), 39-42 (MSSP) and 43 (Reset). Added Date Code information to new issues from revision C (issues 24-33).

### Rev E Document (8/2007)

Added silicon issue 44 (10-Bit A/D Converter). Corrected device IDs.

### Rev F Document (12/2014)

Added silicon issue 22 (Timer1/3).

---

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC<sup>32</sup> logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2004-2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63276-854-4

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC<sup>®</sup> MCUs and dsPIC<sup>®</sup> DSCs, KEELOQ<sup>®</sup> code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*





# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Austin, TX

Tel: 512-257-3370

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Cleveland

Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Novi, MI  
Tel: 248-848-4000

#### Houston, TX

Tel: 281-894-5983

#### Indianapolis

Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### New York, NY

Tel: 631-435-6000

#### San Jose, CA

Tel: 408-735-9110

#### Canada - Toronto

Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2943-5100  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Chongqing

Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

#### China - Hangzhou

Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

#### China - Hong Kong SAR

Tel: 852-2943-5100  
Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

#### China - Xiamen

Tel: 86-592-2388138  
Fax: 86-592-2388130

#### China - Zhuhai

Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-3019-1500

#### Japan - Osaka

Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

#### Japan - Tokyo

Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870  
Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-5778-366  
Fax: 886-3-5770-955

#### Taiwan - Kaohsiung

Tel: 886-7-213-7830

#### Taiwan - Taipei

Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Dusseldorf

Tel: 49-2129-3766400

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Germany - Pforzheim

Tel: 49-7231-424750

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Italy - Venice

Tel: 39-049-7625286

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Poland - Warsaw

Tel: 48-22-3325737

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### Sweden - Stockholm

Tel: 46-8-5090-4654

#### UK - Wokingham

Tel: 44-118-921-5800  
Fax: 44-118-921-5820

03/25/14