# Si53301

# 1:6 Low Jitter Universal Buffer/Level Translator with 2:1 Input Mux

## Features

- 6 differential or 12 LVCMOS outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: 1 to 725 MHz
- Universal any-format input with pin selectable output formats
- LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 input mux
- Glitchless input clock switching
- Synchronous output enable
- Output clock division: /1, /2, /4
- Loss of signal (LOS) monitors for loss of input clock
- Independent $V_{DD}$ and $V_{DDO}$ : 1.8/2.5/3.3 V
- 1.2/1.5 V LVCMOS output support
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 32-QFN (5 mm x 5 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C

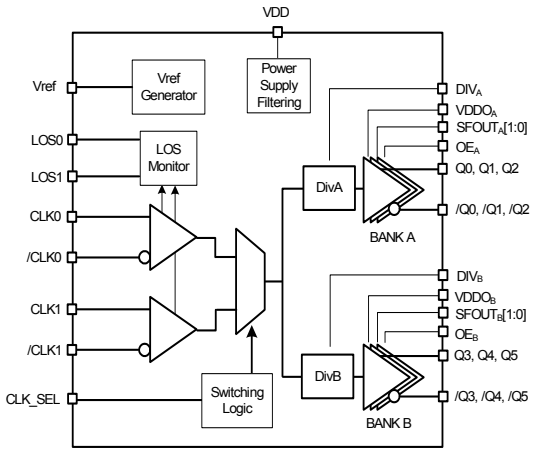
## Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

## Description

The Si53301 is an ultra low jitter six output differential buffer with pin-selectable output clock signal format and divider selection. The Si53301 features a 2:1 input mux with glitchless switching, making it ideal for redundant clocking applications. The Si53301 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53301 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

## Functional Block Diagram

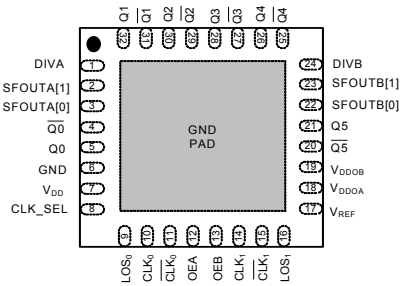


**Ordering Information:**

See page 29.

**Pin Assignments**

**Si53301**




Patents pending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# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | | –40 | — | 85 | °C |
| Supply Voltage Range* | $V_{DD}$ | LVDS, CML | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVCMOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |
| Output Buffer Supply Voltage* | $V_{DDOX}$ | LVDS, CML, LVCMOS | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |

***Note:** Core supply $V_{DD}$ and output buffer supplies $V_{DDO}$ are independent. LVCMOS clock input is not supported for $V_{DD}$ = 1.8V but is supported for LVCMOS clock output for $V_{DDOX}$ = 1.8V. LVCMOS outputs at 1.5V and 1.2V can be supported via a simple resistor divider network. See “2.11.1. LVCMOS Output Termination To Support 1.5V and 1.2V”

### Table 2. Input Clock Specifications

($V_{DD}$=1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$=–40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential Input Common Mode Voltage | $V_{CM}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | 0.05 | — | — | V |
| Differential Input Swing (peak-to-peak) | $V_{IN}$ | | 0.2 | — | 2.2 | V |
| LVCMOS Input High Voltage | $V_{IH}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | $V_{DD}$ x 0.7 | — | — | V |
| LVCMOS Input Low Voltage | $V_{IL}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | — | — | $V_{DD}$ x 0.3 | V |
| Input Capacitance | $C_{IN}$ | CLK0 and CLK1 pins with respect to GND | — | 5 | — | pF |

### Table 3. DC Common Characteristics

($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | — | 65 | 100 | mA |
| Output Buffer Supply Current (Per Clock Output) @100 MHz (diff) @200 MHz (CMOS) | $I_{DDOX}$ | LVPECL (3.3 V) | — | 35 | — | mA |
| | | Low Power LVPECL (3.3 V)* | — | 35 | — | mA |
| | | LVDS (3.3 V) | — | 20 | — | mA |
| | | CML (3.3 V) | — | 35 | — | mA |
| | | HCSL, 100 MHz, 2 pF load (3.3 V) | — | 35 | — | mA |
| | | CMOS (1.8 V, SFOUT = Open/0), per output, $C_L$ = 5 pF, 200 MHz | — | 5 | — | mA |
| | | CMOS (2.5 V, SFOUT = Open/0), per output, $C_L$ = 5 pF, 200 MHz | — | 8 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L$ = 5 pF, 200 MHz | — | 15 | — | mA |
| Input Clock Voltage Reference | $V_{REF}$ | $V_{REF}$ pin $I_{REF}$ = +/-500 µA | — | VDD/2 | — | V |
| Input High Voltage | $V_{IH}$ | SFOUTx, DIVx CLK_SEL, OEx | 0.8 x VDD | — | — | V |
| Input Mid Voltage | $V_{IM}$ | SFOUTx, DIVx 3-level input pins | 0.45 x VDD | 0.5 x VDD | 0.55 x VDD | V |
| Input Low Voltage | $V_{IL}$ | SFOUTx, DIVx CLK_SEL, OEx | — | — | 0.2 x VDD | V |
| Output Voltage High (LOSx) | $V_{OH}$ | $I_{DD}$ = –1 mA | 0.8xVDD | — | — | V |
| Output Voltage Low (LOSx) | $V_{OL}$ | $I_{DD}$ = 1 mA | — | — | 0.2xVDD | V |
| Internal Pull-down Resistor | $R_{DOWN}$ | CLK_SEL, DIVx, SFOUTx | — | 25 | — | kΩ |
| Internal Pull-up Resistor | $R_{UP}$ | OEx, DIVx, SFOUTx | — | 25 | — | kΩ |

***Note:** Low-power LVPECL mode supports an output termination scheme that will reduce overall system power.

### Table 4. Output Characteristics (LVPECL)
($V_{DDOX}$ = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output DC Common Mode Voltage | $V_{COM}$ | | $V_{DDOX}$ – 1.595 | — | $V_{DDOX}$ – 1.245 | V |
| Single-Ended Output Swing* | $V_{SE}$ | | 0.55 | 0.80 | 1.050 | V |
| ***Note:** Unused outputs can be left floating. Do not short unused outputs to ground. | | | | | | |

### Table 5. Output Characteristics (Low Power LVPECL)
($V_{DDOX}$ = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output DC Common Mode Voltage | $V_{COM}$ | $R_L$ = 100 Ω across Qn and $\overline{Qn}$ | $V_{DDOX}$ – 1.895 | | $V_{DDOX}$ – 1.275 | V |
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 100 Ω across Qn and $\overline{Qn}$ | 0.25 | 0.60 | 0.85 | V |

### Table 6. Output Characteristics—CML
($V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | Terminated as shown in Figure 9 (CML termination). | 300 | 400 | 550 | mV |

### Table 7. Output Characteristics—LVDS
($V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 247 | — | 490 | mV |
| Output Common Mode Voltage ($V_{DDO}$ = 2.5 V or 3.3V) | $V_{COM1}$ | $V_{DDOX}$ = 2.38 to 2.63 V, 2.97 to 3.63 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 1.10 | 1.25 | 1.35 | V |
| Output Common Mode Voltage ($V_{DDO}$ = 1.8 V) | $V_{COM2}$ | $V_{DDOX}$ = 1.71 to 1.89 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 0.85 | 0.97 | 1.25 | V |

### Table 8. Output Characteristics—LVCMOS

($V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High* | $V_{OH}$ | | 0.75 x $V_{DDOX}$ | — | — | V |
| Output Voltage Low* | $V_{OL}$ | | — | — | 0.25 x $V_{DDOX}$ | V |
| ***Note:** $I_{OH}$ and $I_{OL}$ per the Output Signal Format Table for specific $V_{DDOX}$ and SFOUTX settings. | | | | | | |

### Table 9. Output Characteristics—HCSL

($V_{DDOX}$ = 3.3 V ± 10%, $T_A$ = –40 to 85 °C))

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High | $V_{OH}$ | $R_L$ = 50 Ω to GND | 550 | 700 | 900 | mV |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 50 Ω to GND | –150 | 0 | 150 | mV |
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 50 Ω to GND | 550 | 700 | 850 | mV |
| Crossing Voltage | $V_C$ | $R_L$ = 50 Ω to GND | 250 | 350 | 550 | mV |

### Table 10. AC Characteristics

($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LOSx Clear Time | $T_{LOSCLR}$ | F < 100 MHz | — | Tper+15 | — | ns |
| | | F > 100 MHz | — | 25 | — | ns |
| LOSx Activation Time | $T_{LOSACT}$ | | — | 15 | — | µs |
| Frequency | F | LVPECL, low power LVPECL, LVDS, CML, HCSL | 1 | — | 725 | MHz |
| | | LVCMOS | 1 | — | 200 | MHz |
| Duty Cycle<br>**Note:** 50% input duty cycle. | $D_C$ | 200 MHz, 20/80% $T_R/T_F$<10% of period (LVCMOS) (12 mA drive) | 40 | 50 | 60 | % |
| | | 20/80% $T_R/T_F$<10% of period (Differential) | 48 | 50 | 52 | % |

**Notes:**

1. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
2. HCSL measurements were made with receiver termination. See Figure 9 on page 19.
3. Output to Output skew specified for outputs with an identical configuration.
4. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
5. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 10. AC Characteristics (Continued)**
($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Minimum Input Clock Slew Rate[1] | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |
| Output Rise/Fall Time | $T_R/T_F$ | LVDS, 20/80% | — | — | 325 | ps |
| | | LVPECL, 20/80% | — | — | 350 | ps |
| | | HCSL[2], 20/80% | — | — | 280 | ps |
| | | CML, 20/80% | — | — | 350 | ps |
| | | Low-Power LVPECL, 20/80% | — | — | 325 | ps |
| | | LVCMOS 200 MHz, 20/80%, 2 pF load | — | — | 750 | ps |
| Minimum Input Pulse Width | $T_W$ | | 500 | — | — | ps |
| Propagation Delay | $T_{PLH}$, $T_{PHL}$ | LVCMOS (12mA drive with no load) | 1250 | 2000 | 2750 | ps |
| | | LVPECL, LVDS | 600 | 800 | 1000 | ps |
| Output Enable Time | $T_{EN}$ | F = 1 MHz | — | 2500 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Disable Time | $T_{DIS}$ | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output to Output Skew[3] | $T_{SK}$ | LVCMOS (12 mA drive to no load) | — | 50 | 120 | ps |
| | | LVPECL | — | 35 | 70 | ps |
| | | LVDS | — | 35 | 70 | ps |
| Part to Part Skew[4] | $T_{PS}$ | Differential | — | — | 150 | ps |

**Notes:**
1. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
2. HCSL measurements were made with receiver termination. See Figure 9 on page 19.
3. Output to Output skew specified for outputs with an identical configuration.
4. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
5. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 10. AC Characteristics (Continued)**
($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Noise Rejection[5] | PSRR | 10 kHz sinusoidal noise | — | –65 | — | dBc |
| | | 100 kHz sinusoidal noise | — | –63 | — | dBc |
| | | 500 kHz sinusoidal noise | — | –60 | — | dBc |
| | | 1 MHz sinusoidal noise | — | –55 | — | dBc |

**Notes:**
1. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
2. HCSL measurements were made with receiver termination. See Figure 9 on page 19.
3. Output to Output skew specified for outputs with an identical configuration.
4. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
5. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 11. Additive Jitter, Differential Clock Input**

| $V_{DD}$ | Input[1,2] | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz)[3] | |
|---|---|---|---|---|---|---|---|
| | Freq (MHz) | Clock Format | Amplitude $V_{IN}$ (Single-Ended, Peak-to-Peak) | Differential 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 150 | 200 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 145 | 195 |

**Notes:**
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

### Table 12. Additive Jitter, Single-Ended Clock Input

| $V_{DD}$ | Input[1,2] | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz)[3] | |
|---|---|---|---|---|---|---|---|
| | Freq (MHz) | Clock Format | Amplitude $V_{IN}$ (single-ended, peak to peak) | SE 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 200 | Single-ended | 1.70 | 1 | LVCMOS[4] | 120 | 160 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 150 | 200 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVCMOS[4] | 130 | 180 |
| 2.5 | 200 | Single-ended | 1.70 | 1 | LVCMOS[5] | 120 | 160 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 145 | 195 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVCMOS[5] | 140 | 180 |

**Notes:**
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11). LVCMOS jitter is measured single-ended.
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11). LVCMOS jitter is measured single-ended.

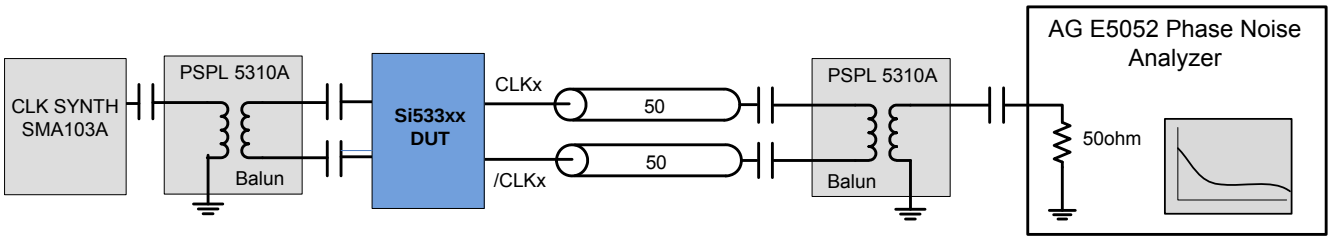



**Figure 1. Differential Measurement Method Using a Balun**

### Table 13. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $\theta_{JA}$ | Still air | 49.6 | °C/W |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | Still air | 32.3 | °C/W |

### Table 14. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | | –55 | — | 150 | °C |
| Supply Voltage | $V_{DD}$ | | –0.5 | — | 3.8 | V |
| Input Voltage | $V_{IN}$ | | –0.5 | — | $V_{DD}$+ 0.3 | V |
| Output Voltage | $V_{OUT}$ | | — | — | $V_{DD}$+ 0.3 | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 kΩ | — | — | 2000 | V |
| ESD Sensitivity | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | $T_{PEAK}$ | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | $T_J$ | | — | — | 125 | °C |

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

# 2. Functional Description

The Si53301 is a low jitter, low skew 1:6 differential buffer with an integrated 2:1 input mux. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin is used to select the active input clock. The selected clock input is routed to two independent banks of three differential clock outputs (Bank A and Bank B). Each output bank features control pins to select signal format, output enable, output divider setting and LVCMOS drive strength.

## 2.1. Universal, Any-Format Input

The Si53301 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increased the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

**Table 15. LVPECL, LVCMOS, and LVDS Input Clock Options**

| | LVPECL | | LVCMOS | | LVDS | |
|---|---|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | N/A | N/A | No | No | Yes | No |
| 2.5/3.3 V | Yes | Yes | No | Yes | Yes | Yes |

**Table 16. HCSL and CML Input Clock Options**

| | HCSL | | CML | |
|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | No | No | Yes | No |
| 2.5/3.3 V | Yes (3.3 V) | Yes (3.3 V) | Yes | No |

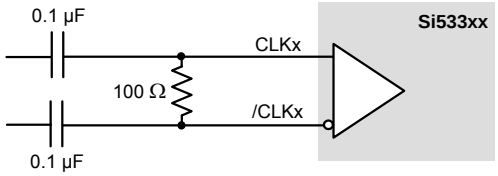



**Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination**

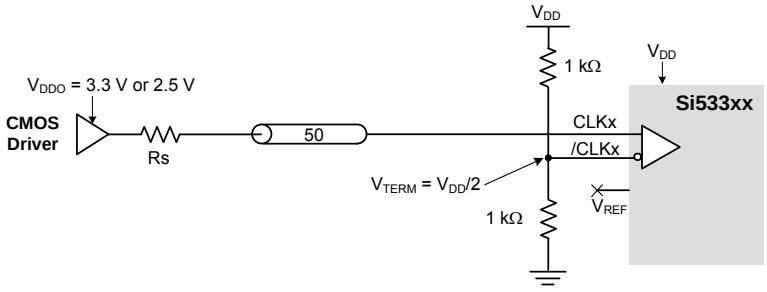
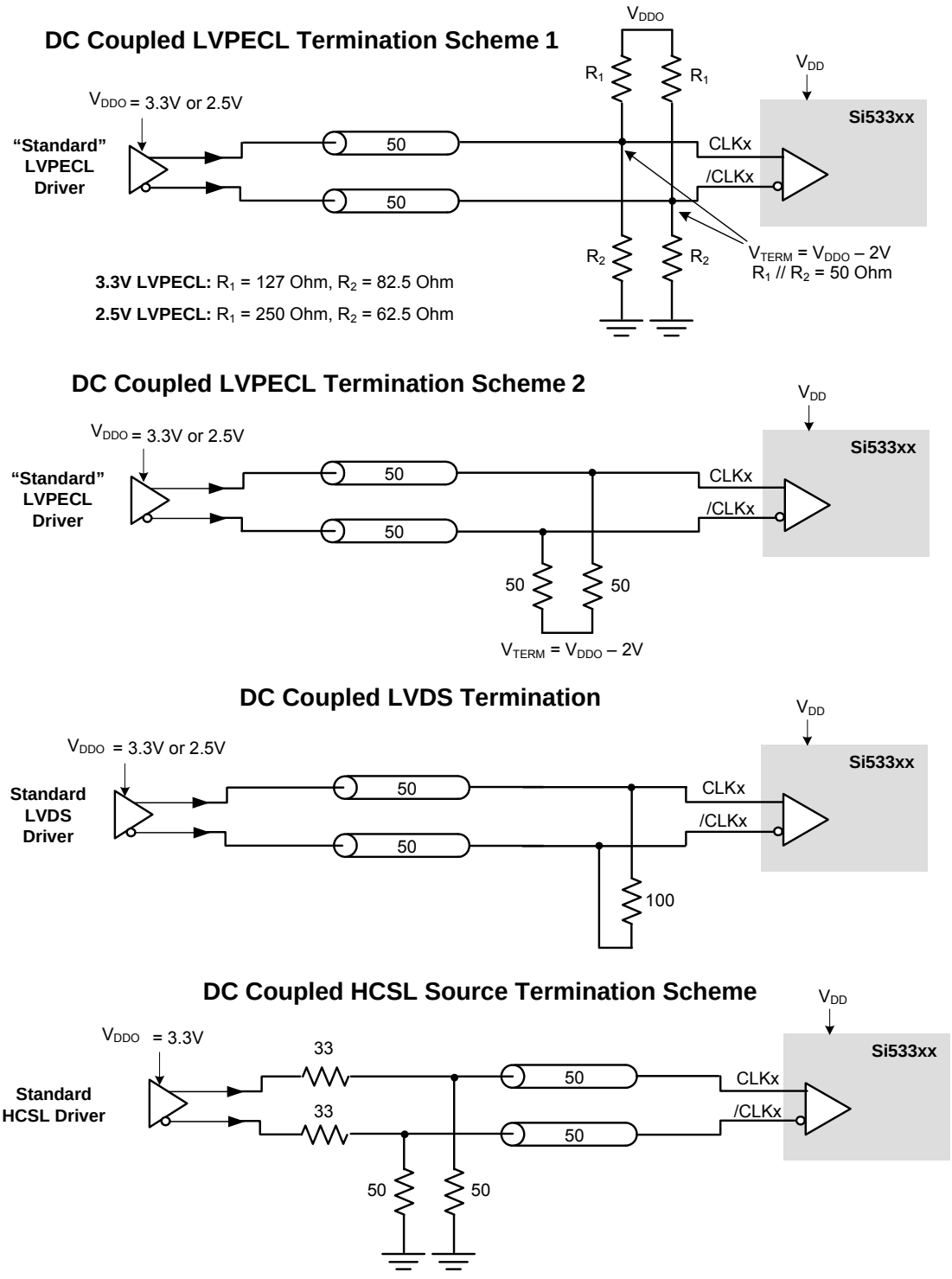



**Figure 3. LVCMOS DC-Coupled Input Termination**




Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 4. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 kΩ pull-down to GND and a 75 kΩ pull-up to $V_{DD}$. The inverting input is biased with a 75 kΩ pull-up to $V_{DD}$.

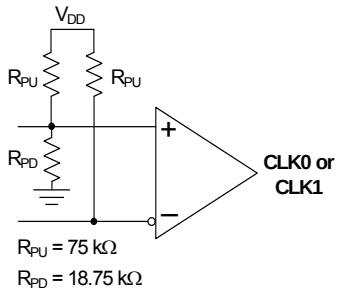



**Figure 5. Input Bias Resistors**

## 2.3. Input Clock Voltage Reference ($V_{REF}$)

The VREF pin is used to bias the input receiver when a differential input clock is terminated as a single-ended reference clock to the device. Connect the single-ended input to either CLK0 or CLK1. Use the recommended input termination and bias circuit as shown in Figure 3. Note that the VREF pin should be left floating when LVCMOS or differential reference clocks are used.

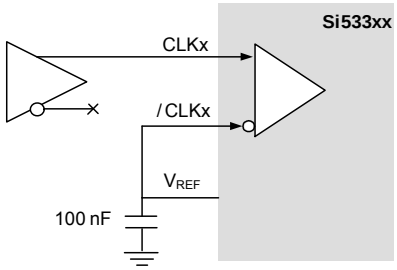



**Figure 6. Using Voltage Reference with Single-Ended Input Clock**

## 2.4. Universal, Any-Format Output Buffer

The Si53301 has highly flexible output drivers that support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTX[1] and SFOUTX[0] are 3-level inputs that can be pin-strapped to select the Bank A and Bank B clock signal formats independently. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each $V_{DDO}$ setting.

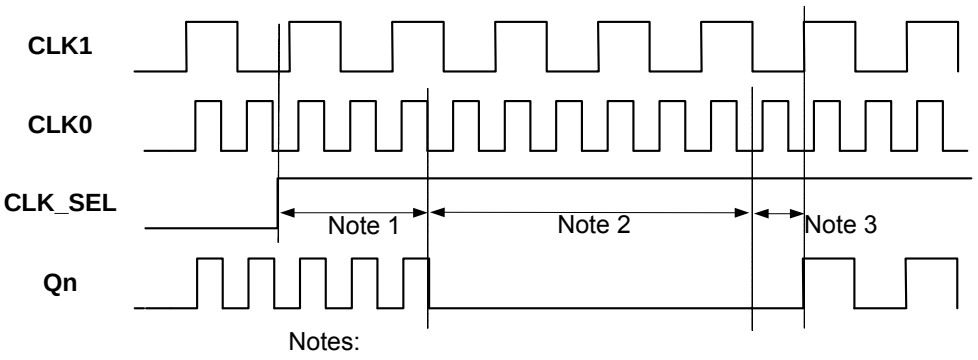
**Table 17. Output Signal Format Selection**

| SFOUTX[1] | SFOUTX[0] | $V_{DDOX}$ = 3.3 V | $V_{DDOX}$ = 2.5 V | $V_{DDOX}$ = 1.8 V |
|---|---|---|---|---|
| Open* | Open* | LVPECL | LVPECL | N/A |
| 0 | 0 | LVDS | LVDS | LVDS |
| 0 | 1 | LVCMOS, 24 mA drive | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive |
| 1 | 0 | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive |
| 1 | 1 | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive | LVCMOS, 6 mA drive |
| Open* | 0 | LVCMOS, 6 mA drive | LVCMOS, 4 mA drive | LVCMOS, 2 mA drive |
| Open* | 1 | LVPECL low power | LVPECL low power | N/A |
| 0 | Open* | CML | CML | CML |
| 1 | Open* | HCSL | N/A | N/A |

***Note:** SFOUTX are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to $V_{DD}/2$.

## 2.5. Glitchless Clock Input Switching

The Si53301 features glitchless switching between two valid input clocks. Figure 7 illustrates that switching between input clocks does not generate runt pulses or glitches at the output.




Notes:

1. $Q_n$ continues with CLK0 for 2-3 falling edges of CLK0.
2. $Q_n$ is disabled low for 2-3 falling edges of CLK1 .
3. $Q_n$ starts on the first rising edge after 1 + 2.

**Figure 7. Glitchless Input Clock Switch**

The Si53301 supports glitchless switching between clocks at the same frequency. In addition, the device supports glitchless switching between 2 input clocks that are up to 10x different in frequency. When a switchover to a new clock is made, the output will disable low after two or three clock cycles of the previously-selected input clock. The outputs will remain low for up to three clock cycles of the newly-selected clock, after which the outputs will start from the newly-selected input. In the case a switchover to an absent clock is made, the output will glitchlessly stop low and wait for edges of the newly selected clock. A switchover from an absent clock to a live clock will also be glitchless. Note that the CLK_SEL input should not be toggled faster than 1/250th the frequency of the slower input clock.

## 2.6. Synchronous Output Enable

The Si53301 features a synchronous output enable (disable) feature. The output enable pin is sampled and synchronized to the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats. For LVCMOS output format options, both Q and $\overline{Q}$ are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected. See Table 10, “AC Characteristics,” on page 6 for output enable and output disable times.

## 2.7. Flexible Output Divider

The Si53301 provides optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVx pins open will force a divider value of 1 which is the default mode of operation. Note that when using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.

**Table 18. Post Divider Selection**

| DIVx | Divider Value |
|---|---|
| Open* | ÷1 (default) |
| 0 | ÷2 |
| 1 | ÷4 |
| ***Note:** DIVx are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to VDD/2. | |

## 2.8. Input Mux and Output Enable Logic

The Si53301 provides two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

**Table 19. Input Mux and Output Enable Logic**

| CLK_SEL | CLK0 | CLK1 | OE[1] | Q[2] |
|---|---|---|---|---|
| L | L | X | H | L |
| L | H | X | H | H |
| H | X | L | H | L |
| H | X | H | H | H |
| X | X | X | L | L[3] |

**Notes:**
1. Output enable active high
2. On the next negative transition of CLK0 or CLK1.
3. Single-end: Q = low, $\overline{Q}$ = low
   Differential: Q = low, $\overline{Q}$ = high

## 2.9. Loss of Signal (LOS) Indicator

The LOS0 and LOS1 indicators are used to check for the presence of input clocks CLK0 and CLK1. The LOS0 and LOS1 pins are checked prior to selecting that clock input or are polled to check for the presence of the currently selected input clock. In the event that an input clock is not present, the associated LOSx pin will assume a logic high (LOSx = 1) state. When a clock is present at the associated input clock pin, the LOSx pin will assume a logic low (LOSx = 0) state.

## 2.10. Power Supply ($V_{DD}$ and $V_{DDOX}$)

The device includes separate core ($V_{DD}$) and output driver supplies ($V_{DDOX}$). This feature allows the core to operate at a lower voltage than $V_{DDO}$, reducing current consumption in mixed supply applications. The core $V_{DD}$ supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own $V_{DDOX}$ supply, supporting 3.3 V, 2.5 V, or 1.8 V.

## 2.11. Output Clock Termination Options

The recommended output clock termination options are shown below.

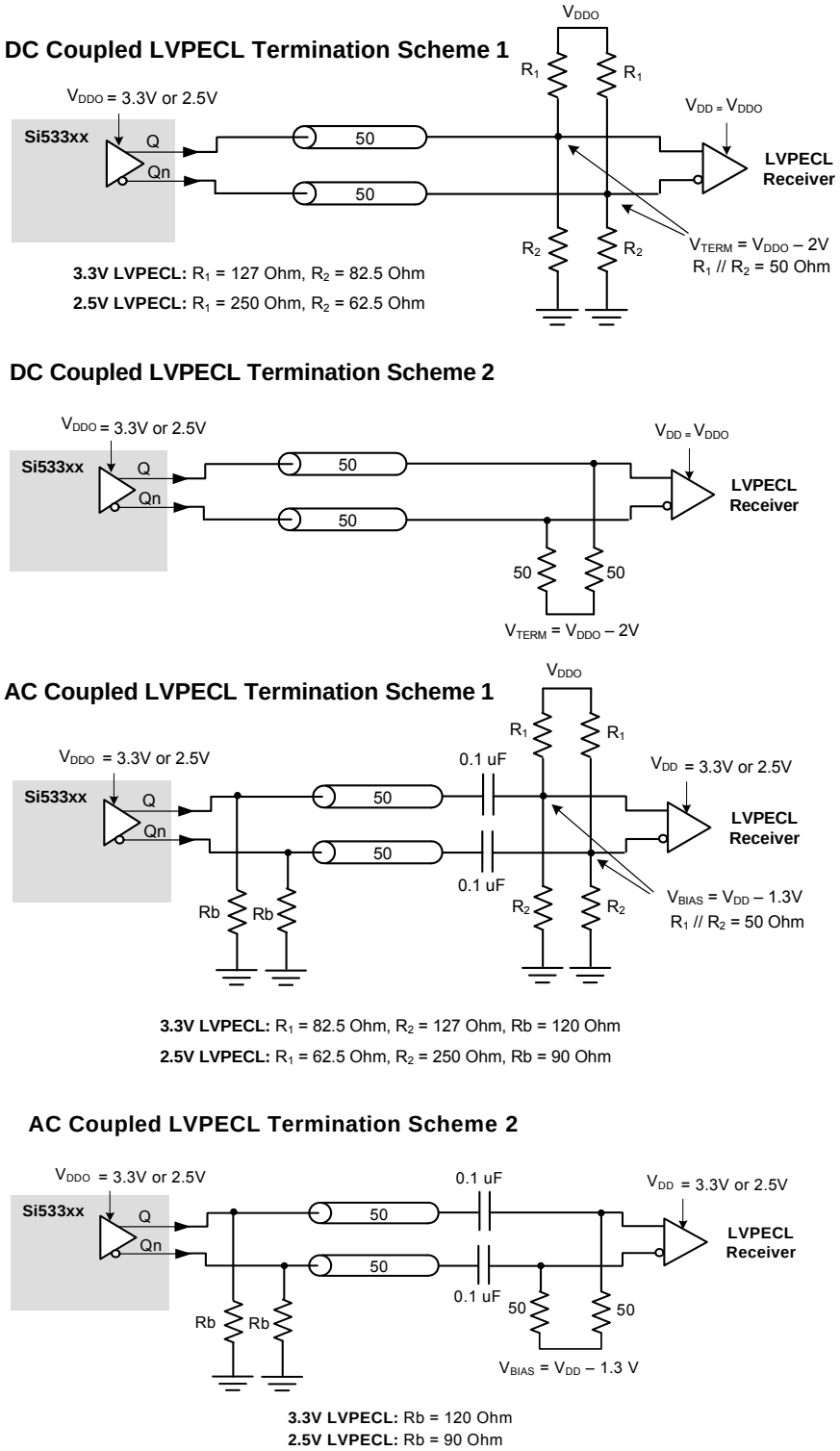



**Figure 8. LVPECL Output Termination**

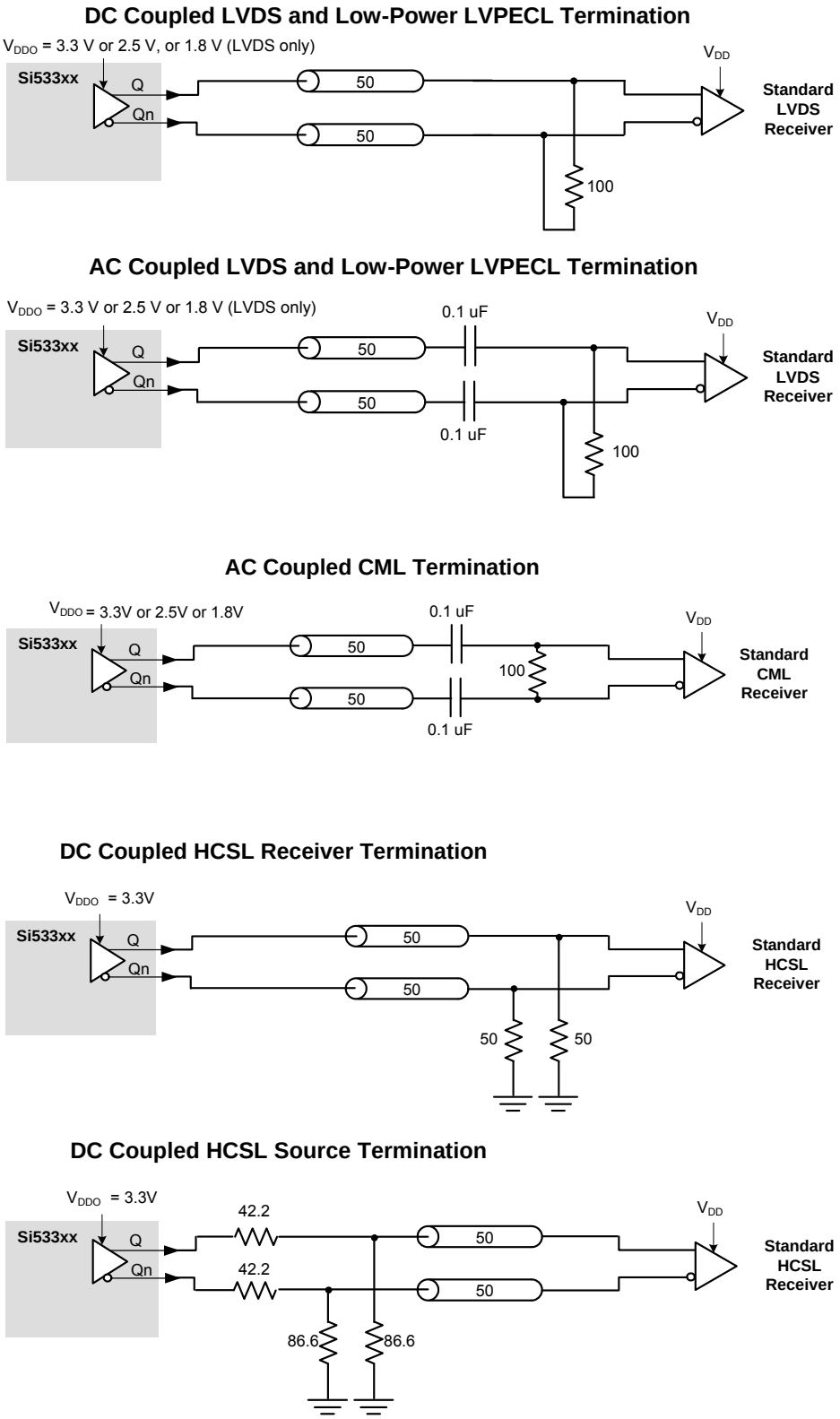



**Figure 9. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination**

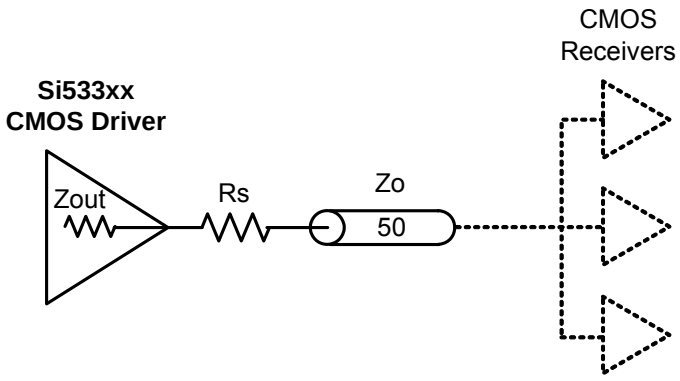



**Figure 10. LVCMOS Output Termination**

**Table 20. Recommended LVCMOS $R_S$ Series Termination**

| SFOUTX[1] | SFOUTX[0] | $R_S$ (ohms) | | |
|---|---|---|---|---|
| | | 3.3 V | 2.5 V | 1.8 V |
| 0 | 1 | 33 | 33 | 33 |
| 1 | 0 | 33 | 33 | 33 |
| 1 | 1 | 33 | 33 | 0 |
| Open | 0 | 0 | 0 | 0 |

### 2.11.1. LVCMOS Output Termination To Support 1.5V and 1.2V

LVCMOS clock outputs are natively supported at 1.8, 2.5, and 3.3V. However, 1.2V and 1.5V LVCMOS clock outputs can be supported via a simple resistor divider network that will translate the buffer's 1.8V output to a lower voltage as shown in Figure 11 below.

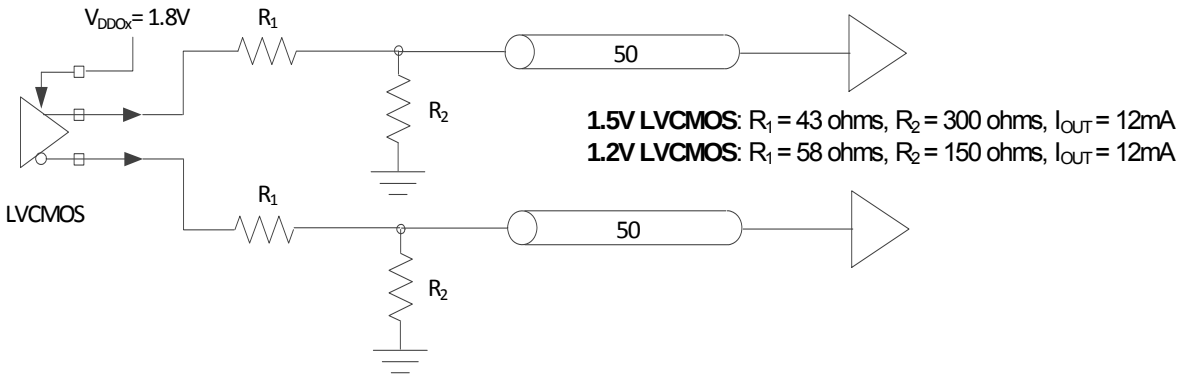



**Figure 11. 1.5V and 1.2V LVCMOS Low-Voltage Output Termination**

## 2.12. AC Timing Waveforms

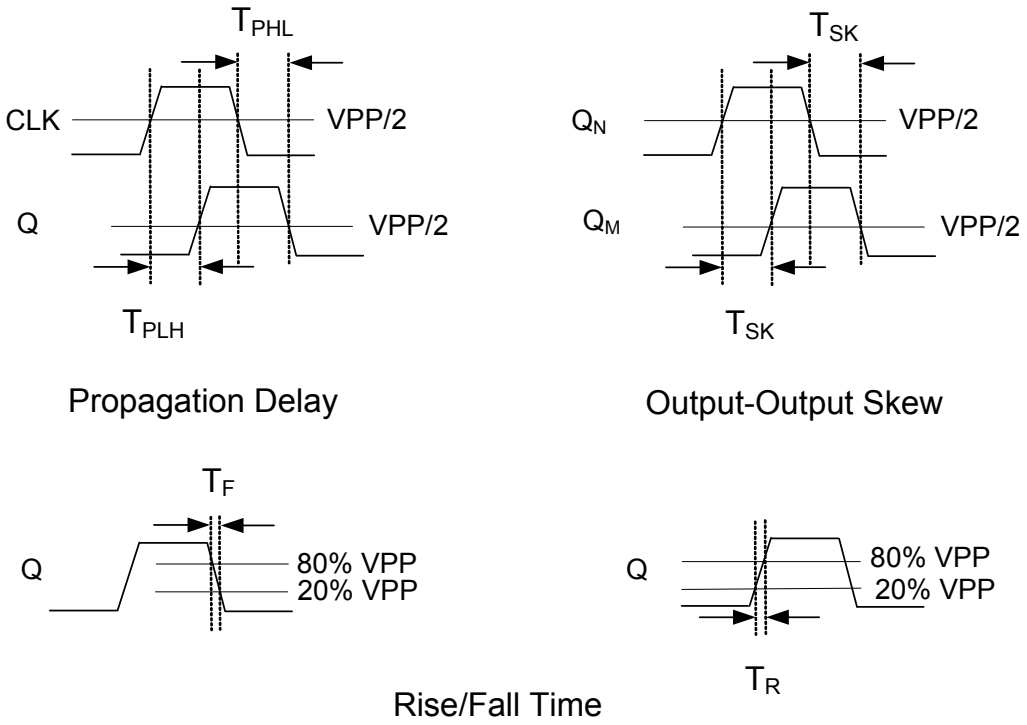



**Figure 12. AC Waveforms**

## 2.13. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

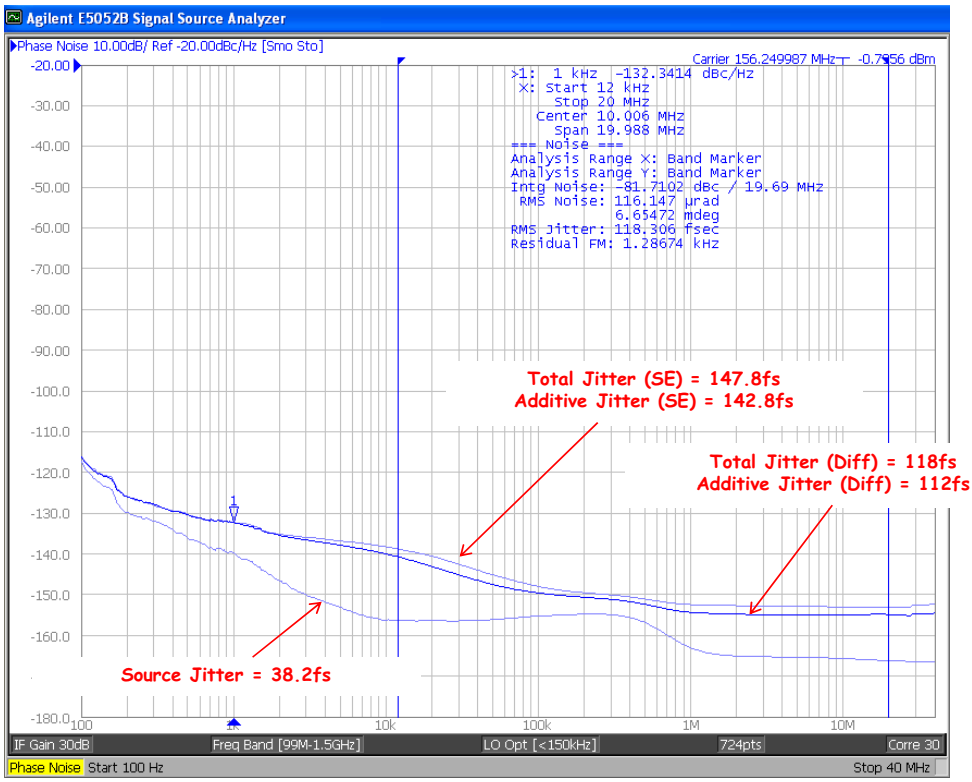
**Source Jitter**: Reference clock phase noise.

**Total Jitter (SE)**: Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

**Total Jitter (Diff)**: Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 10.

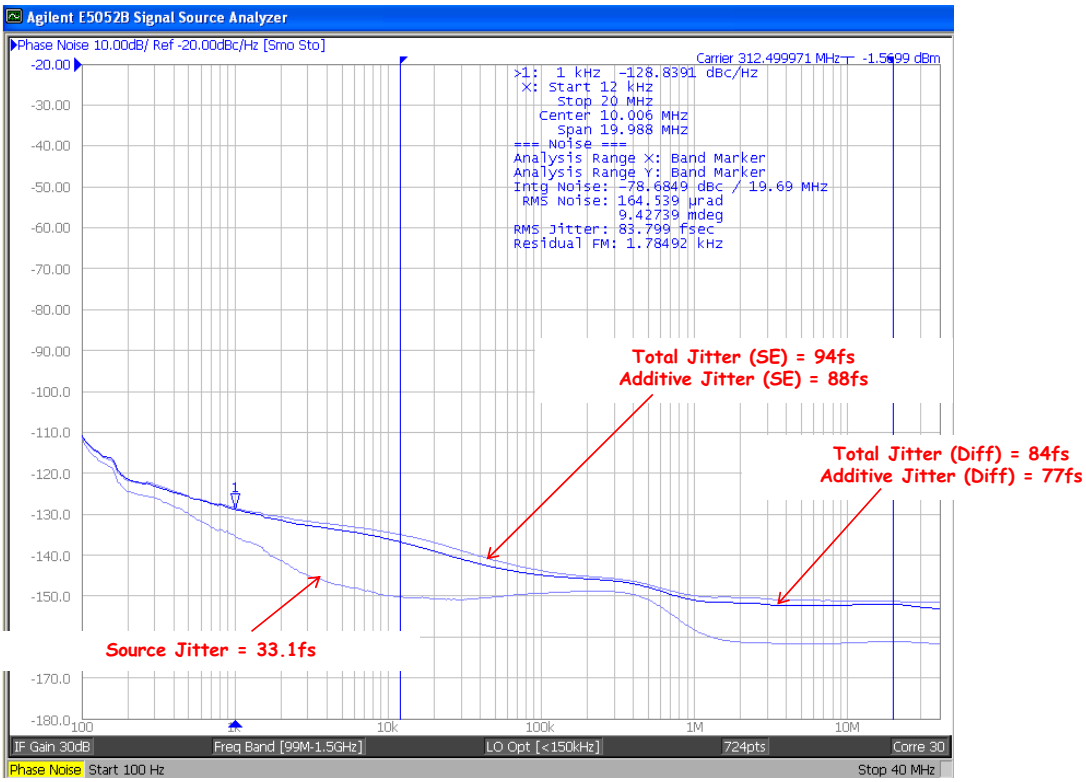
**Note:** To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).




| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff) (fs) | Additive Jitter (Diff) (fs) |
|---|---|---|---|---|---|---|
| 156.25 | 1.0 | 38 | 148 | 143 | 118 | 112 |

**Figure 13. Source Jitter (156.25 MHz)**




| Frequency (MHz) | Diff Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff) (fs) | Additive Jitter (Diff) (fs) |
|---|---|---|---|---|---|---|
| 312.5 | 1.0 | 33 | 94 | 89 | 84 | 77 |

**Figure 14. Single-Ended Total Jitter (312.5 MHz)**

| Frequency (MHz) | Diff Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff) (fs) | Additive Jitter (Diff) (fs) |
|---|---|---|---|---|---|---|
| 625 | 1.0 | 23 | 57 | 52 | 59 | 54 |

**Figure 15. Differential Total Jitter (625 MHz)**

## 2.14. Input Mux Noise Isolation

The input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. Figure 16 below is a measurement the input mux's noise isolation.

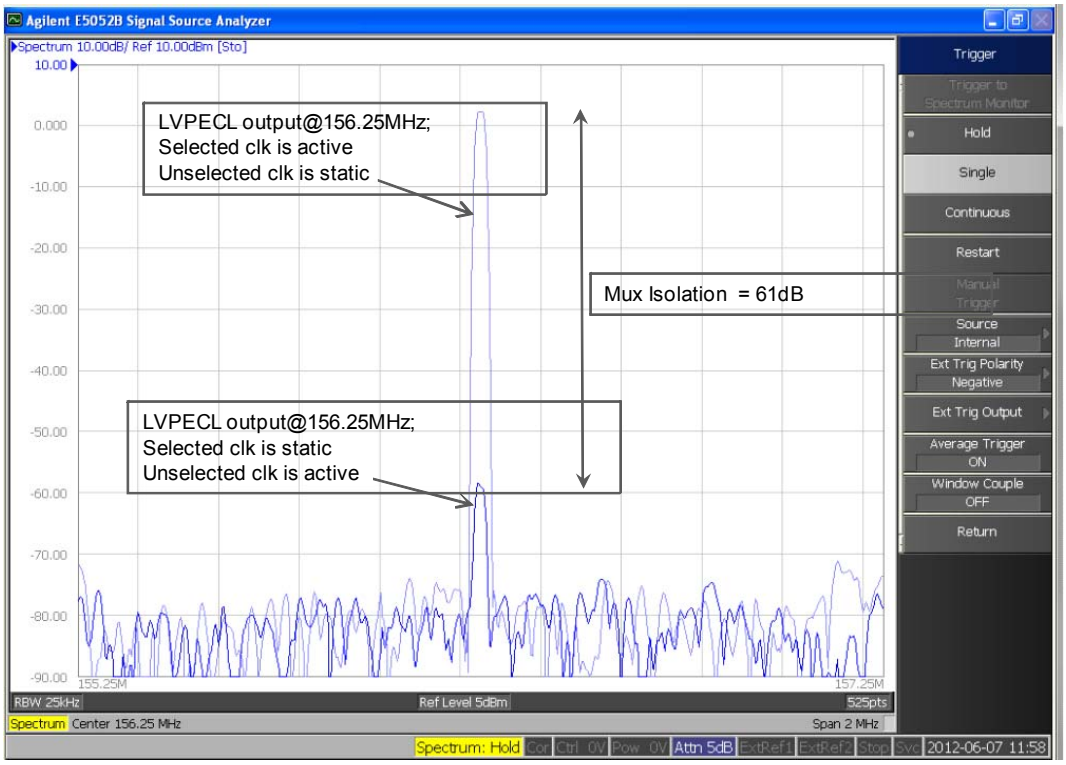



**Figure 16. Input Mux Noise Isolation**

## 2.15. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see "AN491: Power Supply Rejection for Low Jitter Clocks".

## 3. Pin Description: 32-Pin QFN

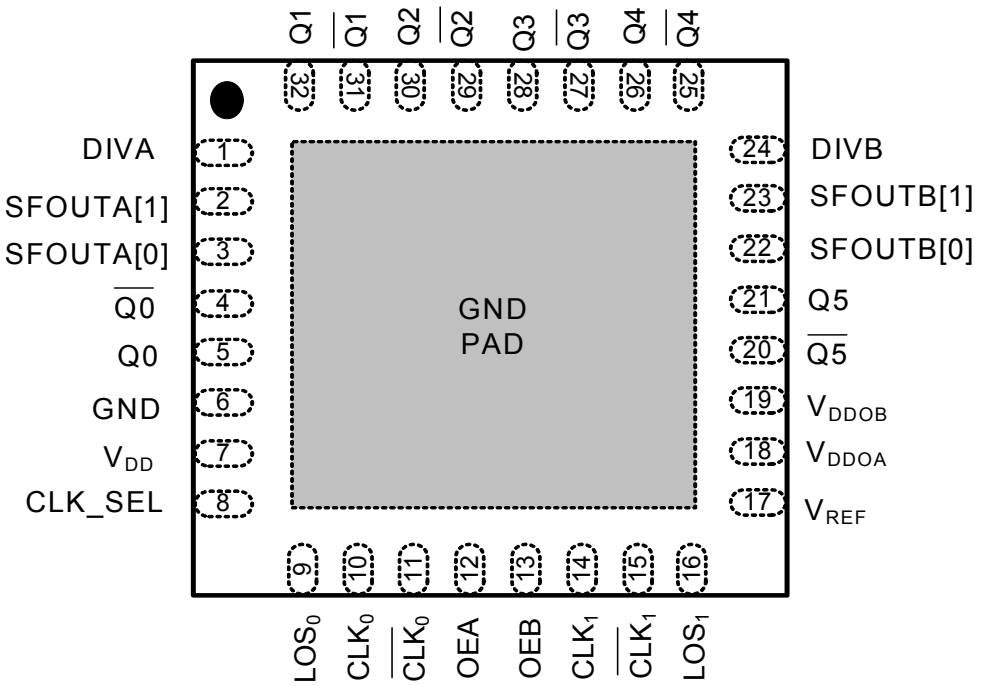



**Table 21. Pin Description**

| Pin | Name | Type* | Description |
|---|---|---|---|
| 1 | DIVA | I | Output divider control pin for Bank A (Outputs: Q0 to Q2)<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 2 | SFOUTA[1] | I | Output signal format control pin for Bank A (Outputs: Q0 to Q2)<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 3 | SFOUTA[0] | I | Output signal format control pin for Bank A (Outputs: Q0 to Q2)<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 4 | $\overline{Q0}$ | O | Output clock 0 (complement) |
| 5 | Q0 | O | Output clock 0 |
| 6 | GND | GND | Ground |
| 7 | $V_{DD}$ | P | Core voltage supply.<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DD}$ pin as possible. |

**Table 21. Pin Description (Continued)**

| Pin | Name | Type* | Description |
|---|---|---|---|
| 8 | CLK_SEL | I | Mux input select pin:<br>Clock inputs are switched without the introduction of glitches.<br>When CLK_SEL is high, CLK1 is selected.<br>When CLK_SEL is low, CLK0 is selected.<br>CLK_SEL contains an internal pull-down resistor. |
| 9 | LOS0 | O | The LOS0 status pin indicates whether a clock is present at the CLK0 pin:<br>CLK0 input clock present LOS0 = 0<br>CLK0 input clock not present LOS0 = 1 |
| 10 | CLK0 | I | Input clock 0 |
| 11 | $\overline{CLK0}$ | I | Input clock 0 (complement). |
| 12 | OEA | I | Output enable—Bank A (Outputs: Q0 to Q2)<br>When OE = high, the Bank A outputs are enabled.<br>When OE = low, Q is held low, and $\overline{Q}$ is held high for differential formats.<br>For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low.<br>OEA features an internal pull-up resistor and may be left unconnected. |
| 13 | OEB | I | Output enable—Bank B (Outputs: Q3 to Q5)<br>When OE = high, the Bank B outputs are enabled.<br>When OE = low, Q is held low, and $\overline{Q}$ is held high for differential formats.<br>For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low.<br>OEB features an internal pull-up resistor and may be left unconnected. |
| 14 | CLK1 | I | Input clock 1 |
| 15 | $\overline{CLK1}$ | $\overline{I}$ | Input clock 1 (complement) |
| 16 | LOS1 | O | The LOS1 status pin indicates whether a clock is present at the CLK1 pin:<br>CLK1 input clock present LOS1 = 0<br>CLK1 input clock not present LOS1 = 1 |
| 17 | $V_{REF}$ | O | Input clock reference voltage used to bias CLK0 or CLK1 clock input pins. VREF is required when a differential input clock is applied to the device and terminated as a single-ended reference. VREF may be left unconnected for LVCMOS or differential clock inputs. See section “2.3. Input Clock Voltage Reference (VREF)” for details. |
| 18 | $V_{DDOA}$ | P | Output voltage supply—Bank A (Outputs: Q0 to Q2)<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DDOA}$ pin as possible. |
| 19 | $V_{DDOB}$ | P | Output voltage supply—Bank B (Outputs: Q3 to Q5)<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DDOB}$ pin as possible. |
| 20 | $\overline{Q5}$ | O | Output clock 5 (complement) |
| 21 | Q5 | O | Output clock 5 |

**Table 21. Pin Description (Continued)**

| Pin | Name | Type* | Description |
|---|---|---|---|
| 22 | SFOUTB[0] | I | Output signal format control pin for Bank B (Outputs: Q3 to Q5).<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 23 | SFOUTB[1] | I | Output signal format control pin for Bank B (Outputs: Q3 to Q5).<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 24 | DIVB | I | Output divider control pin for Bank B (Outputs: Q3 to Q5).<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 25 | $\overline{Q4}$ | O | Output clock 4 (complement) |
| 26 | Q4 | O | Output clock 4 |
| 27 | $\overline{Q3}$ | O | Output clock 3 (complement) |
| 28 | Q3 | O | Output clock 3 |
| 29 | $\overline{Q2}$ | O | Output clock 2 (complement) |
| 30 | Q2 | O | Output clock 2 |
| 31 | $\overline{Q1}$ | O | Output clock 1 (complement) |
| 32 | Q1 | O | Output clock 1 |
| GND Pad | GND | GND | Ground Pad.<br>Power supply ground and thermal relief. |
| *Pin types are: I = input, O = output, P = power, GND = ground. | | | |

# 4. Ordering Guide

| Part Number | Package | PB-Free, ROHS-6 | Temperature |
|---|---|---|---|
| Si53301-B-GM | 32-QFN | Yes | –40 to 85 °C |
| Si53301/4-EVB | Evaluation Board | Yes | — |

# 5. Package Outline

## 5.1. 5x5 mm 32-QFN Package Diagram

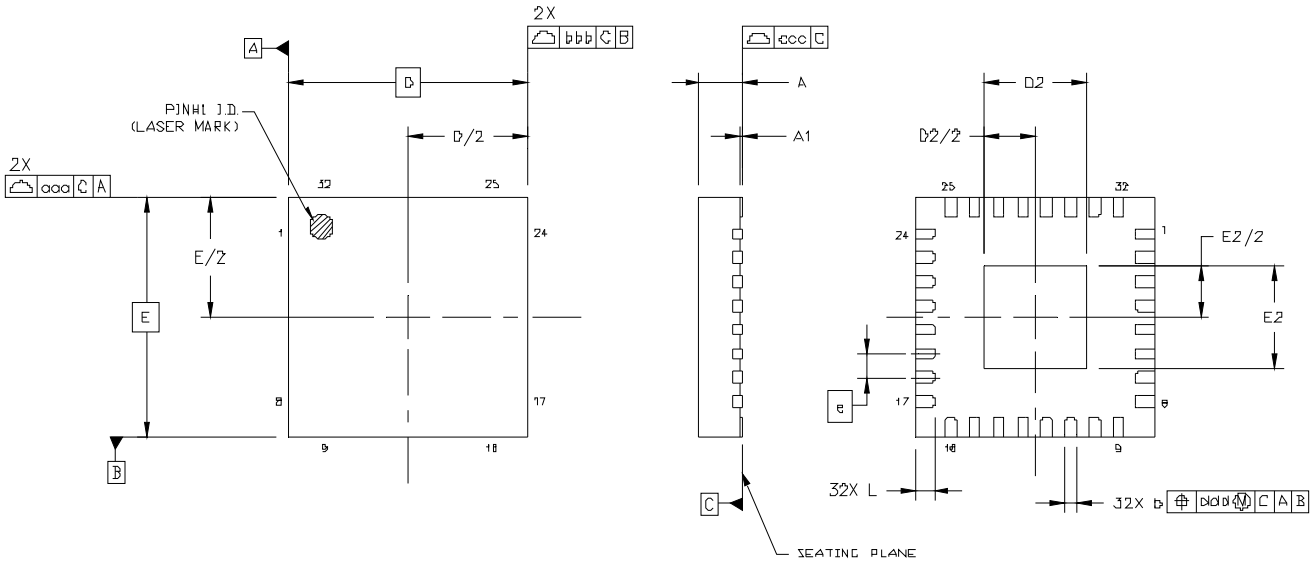



**Figure 17. Si53301 5x5 mm 32-QFN Package Diagram**

**Table 22. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.20 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| D2 | 2.00 | 2.15 | 2.30 |
| e | | 0.50 BSC | |
| E | | 5.00 BSC | |
| E2 | 2.00 | 2.15 | 2.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.10 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.

# 6. PCB Land Pattern

## 6.1. 5x5 mm 32-QFN Package Land Pattern

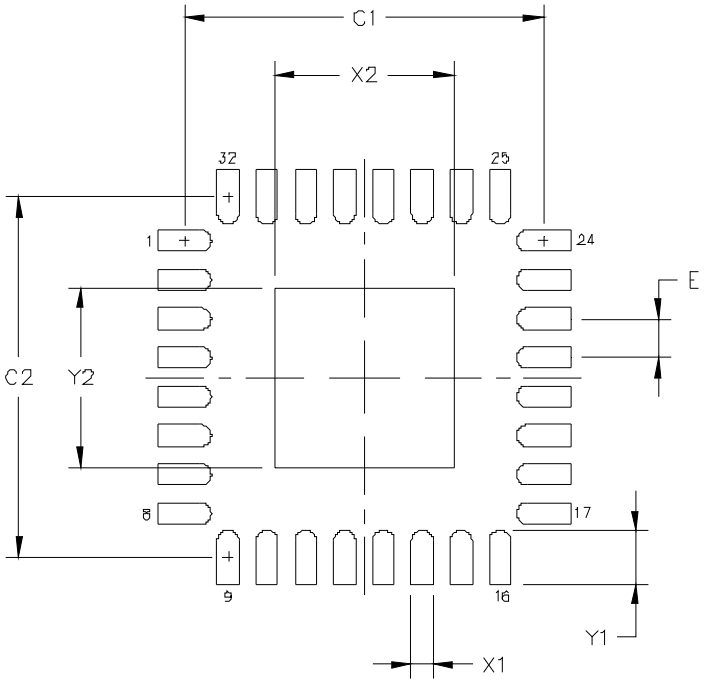



**Figure 18. Si53301 5x5 mm 32-QFN Package Land Pattern**

**Table 23. PCB Land Pattern**

| Dimension | Min | Max |
|---|---|---|
| C1 | 4.52 | 4.62 |
| C2 | 4.52 | 4.62 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |

| Dimension | Min | Max |
|---|---|---|
| X2 | 2.20 | 2.30 |
| Y1 | 0.59 | 0.69 |
| Y2 | 2.20 | 2.30 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

**Stencil Design**

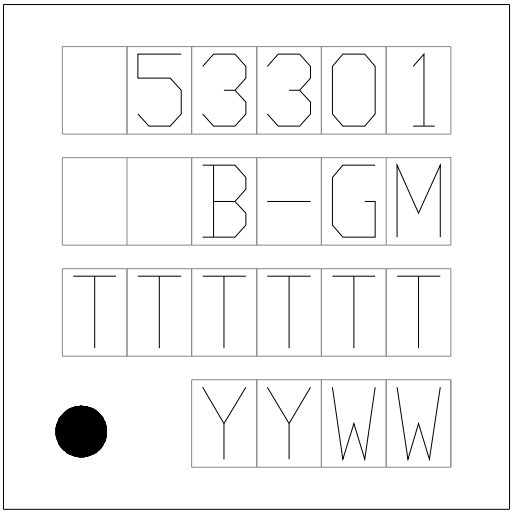
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

**Card Assembly**

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 7. Top Marking

## 7.1. Si53301 Top Marking




## 7.2. Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 2.0 Point (28 mils)<br>Center-Justified | |
| **Line 1 Marking:** | Device Part Number | **53301** |
| **Line 2 Marking:** | Device Revision/Type | **B-GM** |
| **Line 3 Marking:** | TTTTTT | Manufacturing code |
| **Line 4 Marking** | Circle = 0.5 mm Diameter<br>Lower-Left Justified | Pin 1 Identifier |
| | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |

# Document Change List

## Revision 0.4 to Revision 1.0

**Front Page**

- Updates functional block diagram and pin assignment figures to add LOS pins.

**Recommended Operating Conditions**

- Updated Table 1 to clarify notation.
- Spec change: HCSL is supported at 3.3 V only.

**Input Clock Specifications Table**

- Clarification: Input swing spec clarified applies to differential input.
- Clarification: Input voltage high/low spec is for LVCMOS input.
- Clarification: Input capacitance with respect to GND.

**DC Common Characteristics Table**

- Clarification: Denote frequencies for S.E. and Differential outputs for current consumption specs.
- Spec change: Updated Supply/output buffer supply current specs.
- Spec change: LVCMOS is not supported at 1.8 V.
- Spec change: Input high/low voltage levels.
- Correction to show which signals use internal pull-up/pull-down.
- Added specification: Output voltage high/low to support added LOS feature.

**Output Voltage Specifications**

- Spec change: LVPECL and Low-Power LVPECL output voltage level specifications changes.
- Spec change: LVPECL and low-power LVPECL DC characteristics separated into two tables.
- Spec change: LVCMOS logic levels improved.
- Spec change: HCSL single-ended output swing max/min added.

**AC Characteristics**

- Ouput rise/fall time spec test conditions, added low-power LVPECL.
- Duty cycle spec added for LVCMOS, updated differential spec and test conditions.
- Spec change: Propagation delay (was TBD)
- Spec change: Added/expanded output enable/disable time specs for three frequencies.
- Spec change: part to part skew updated.
- Spec chnage: Power supply noise rejection updated.
- Spec change: Improved additive Jitter specification.
- Spec change: Output to output skew updated.
- Updated footnotes.

**Additive Jitter, Differential Clock Input Table**

- Spec changes: Table changed to provide improved specs and add spec previously "TBD" based upon differential measurements.
- Added footnote and test setup Figure 1 for clarity.

**Additive Jitter, Single-Ended Clock Input Table**

- Spec changes: Table changed to provide improved specs and add specs previously "TBD" based upon differential measurements.
- Added footnote and test setup Figure 1 for clarity.

**Pinout Description**

- No pin assignments were moved. Two pins previously indicated as NC have been assigned to the LOS function as follows: Pin 9 is LOS0 and Pin 16 is LOS1.
- Pin assignment and descriptions have been edited to reflect this added feature's pin assignment.
- Correction: Top Marking spec/explanation have been corrected.

**Other Changes**

- Added Figure 1 test setup.
- Input format change: 1.8 V LVCMOS is not supported.
- Clarified support for HCSL is at 3.3 V.
- Updated recommendation in Figure 3 for optimal performance.
- Added dc-coupled receiver termination scheme.
- Output format Selection table reflects LVCMOS (no 1.8 V) and HCSL (3.3 V only).
- Loss of Signal feature is added. Section to describe the loss of signal indicator feature.
- Output termination recommendations: updated to show Low-power LVPECL supported termination.
- Correction: LVCMOS series termination recommendation table.
- Typical phase noise plots updated with improved figures and clearer results.

## Revision 1.0 to Revision 1.1

- Added additional information to clarify the use of the voltage reference feature.
- Added pin type description to the pinout table
- Added low-voltage termination options for 1.2 V and 1.5 V LVCMOS support
- Improved and more detailed performance specifications
- Clarification of output clock bank A and bank B assignments
- Correction to front-page buffer block diagram

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SILICON LABS

**Silicon Laboratories Inc.**
**400 West Cesar Chavez**
**Austin, TX 78701**
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